USER'S MANUAL

PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATOR

PCL5022

NPM NIPPON PULSE MOTOR CO., LTD.

CONTENTS

Considerations in Reading this User's Manual

(1) Varied-speed operation means pulse output with linear acceleration/deceleration at the start/stop.
(2) Constant-speed operation means pulse output at a constant rate with no acceleration/deceleration.
(3) The input/output logic of each pin indicates the logic under the reset condition.
(4) "Plus (+)" in the description indicates incremeting the up/down counter.
(5) "Minus (−)" in the description indicates decrementing the up/down counter.

1. General Description

The PCL5022 is a CMOS LSI. It oscillates high-frequency pulses to drive stepping motors and pulse train input servomotors according to commands transferred through the CPU bus interface. Thus, using this CMOS LSI, you can perform continuous motion control, in-positioning and origin re·rn in various ways including constant speed and linear acceleration/decelera.ion

Furthermore, the CMOS LSI allows you to control two axes, perform simple linear interpolation and check the operation status of PCL5022 as well as letting it oscillate pulses according to an interrupt signal based on conditions.

The PCL5022 is also provided with a function to control servomotor drivers, that accept pulse & direction command.

Our sophisticated design concept lets you easily access to the versatile functions with simple commands while reducing the burden to the CPU.

Features

- Biaxial control
- Linear interpolation (slave axis moves proportionally to main axis)
- Applicable to drivers controlled with microsteps of up to 16 divisions
- Maximum output frequency of 1.2 Mpps with a reference clock of 9.8304MHz
- Out-of-step detection for stepping motor
- Output of idling pulses
- Interface for servomotor control
- External pulse input
- Interface to Intel CPU (connectable with 8 or 16-bit data bus)
- Interface to Motorola CPU (connectable with 8-bit data bus)
- 8-byte address area
- Up/down counter
- Independently selectable acceleration and deceleration rates

2. Specifications

2.1 Specifications

Power Requirement: +5V ±5%

Reference Clock: 9.8304MHz standard (10MHz maximum)

Number of Subject Axes: Two ('a' and 'b' axes)

Number of Positioning Pulses: 0 to 268,435,455

Pulse Rate Setting Steps: 1 to 16,383

Pulse Rate Multiplication Setting Range: 0.05 to 75 times
0.1 to 1,638.3 pps with 0.1x
1 to 16,383 pps with 1x
75 to 1,228,725 pps with 75x

Pulse Rate Setting Registers: Two types of FL and FH

Ramping-down Point Setting Range: 0 to 4,194,303

Acceleration/Deceleration Rate Setting Range: 1 to 16,383

Up/Down Counter Counting Range: 0 to 268,435,455

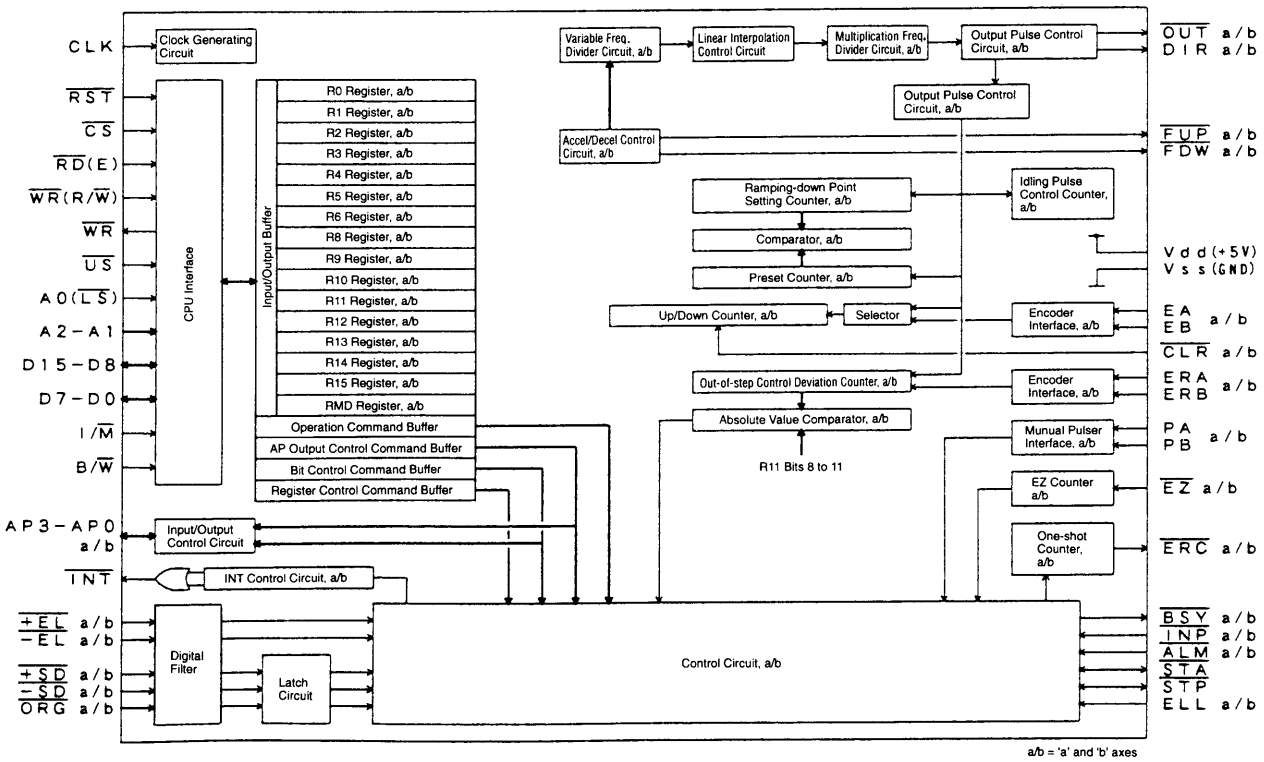
Major Operations Available:
- Continuous operation
- Preset operation
- Origin return
- Timer mode operation
- Linear interpolation

Operating Temperature Range: 0 to +70°C

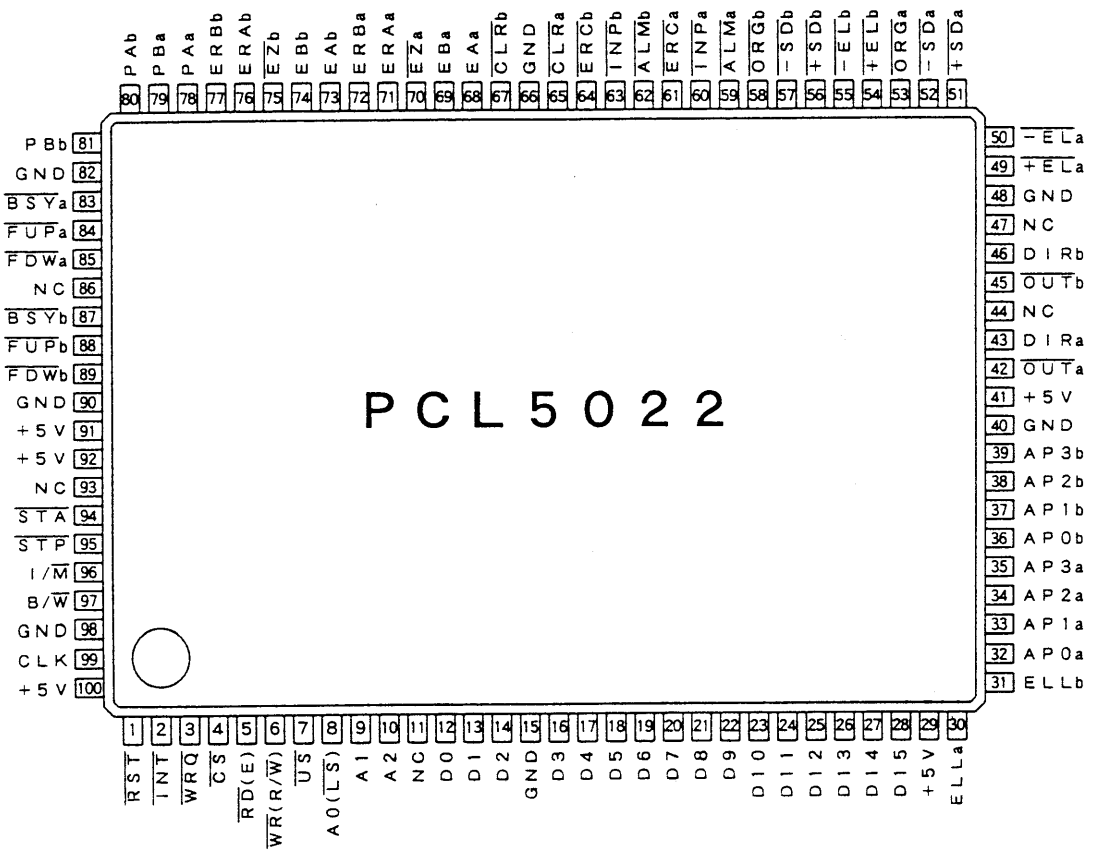
Storage Temperature Range: −40 to +125°C

Package: 100-pin QFP

2.2 Block Diagram



2.3 Terminal Pin Layout

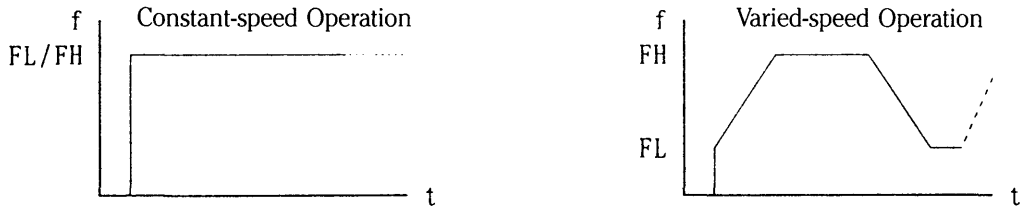


3. Outline of Functions

The PCL5022 starts and stops generating pulses according to commands from the CPU to control two stepping motors or servomotors. By writing desired parameters to the PCL5022, you can control the motors in various ways. This chapter describes terms and the outline of each function. For detailed operation, see the chapter 5.

3.1 Pulse Output Patterns

The PCL5022 allows you to select a pulse output pattern of either constant speed or varied speed.



3.1.1 Constant-speed Operation

The PCL5022 outputs pulses at a fixed frequency to control the motor at a constant speed from the start to end. As the fixed frequency, you can select either the FL pulse rate (low speed) or FH pulse rate (high speed).

3.1.2 Varied-speed Operation

The PCL5022 starts outputting pulses at the FL pulse rate, then accelerates the frequency to the FH pulse rate, which ramps down to the FL rate before termination. Thus, the motor is driven at a high speed with an acceleration at the start and a deceleration at the end.

3.2 Commands

You can operate the PCL5022 by writing commands from the CPU to the designated address (command buffer). There are four basic types of commands. The resultant operations depend on written data.

3.2.1 Start/Stop Commands

Start/stop commands are roughly classified into the following four:

Start command
Stop command
Speed switchover command
Start retention command

The constant-speed or varied-speed operation is selected by writing the data into the command.

3.2.2 AP Output Control Commands

An AP output control command allows you to control the output signal of general-purpose AP input/output pin by bit.

3.2.3 Bit Control Commands

Bit control commands set or reset the internal control circuit. They are roughly classified into the following two:

AP pin bit control command

Reset control command (to set or reset pins, etc.)

3.2.4 Register Control Commands

A register control command allows you to designate the register and read or write the data from/to the register.

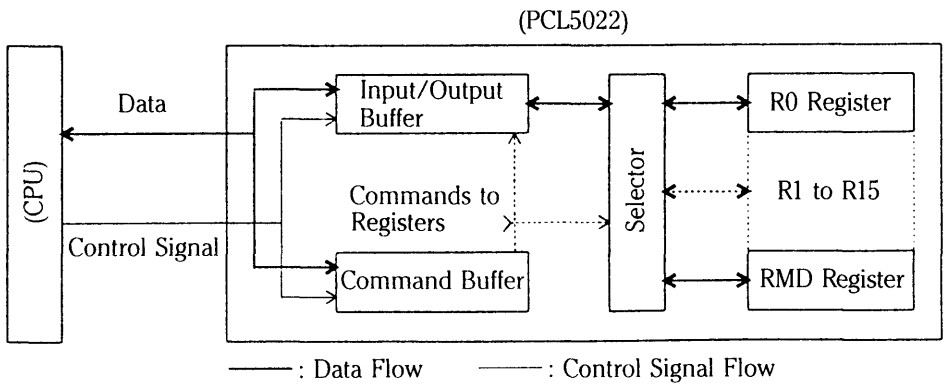
3.3 Registers

Registers store numerical data (pulse rates, number of output pulses, etc.) and control data (direction, operation mode, etc.). The register data are read or written from/to the CPU via the input/output buffer with the register read or register write command.

3.3.1 Input/Output Buffer

The input/output buffer put between the CPU interface and registers temporarily stores register data at the time of reading or writing data from/to the CPU. The register read command lets the input/output buffer read the data once and then the CPU read the data from the input/output buffer. The register write command lets the CPU write the data into the input/output buffer once and then the input/output buffer write the data into a register. The input/output buffer provides a bit length of 32 bits and reads or writes data by dividing it into 8 bits (or 16 bits) while selecting addresses.

Data Flow from/to Registers



3.3.2 Registers Function

The PCL5022 provides registers R0 to R15 and RMD.

R0 Resister, Preset Number of Output Pulses

The R0 register is for the number of output pulses to move the motor in a target amount.

R1 Register, FL Pulse Rate

The R1 register is for the FL pulse rate. In the varied-speed operation, the rate is used at the start of acceleration and at the end of deceleration. Notice that a practical pulse output rate is a product of the rate entered here and a multiplication factor entered in the R5 register.

R2 Register, FH Pulse Rate

The R2 register is the FH pulse rate. In the varied-speed operation, the rate is used in the meantime between acceleration and deceleration. Notice that a practical pulse output rate is a product of the rate entered here and a multiplication factor entered in the R5 register.

R3 Register, Acceleration Rate

The R3 register is for the acceleration rate. The rate is also used for deceleration if the ramping-down point is automatically set for in-positioning.

R4 Register, Deceleration Rate

The R4 register is for the deceleration rate, which is used if the deceleration is not made automatically in the varied-speed operation or in-positioning.

R5 Register, Multiplication Factor

The R5 register is for the multiplication factor which multiplies the pulse rates entered in R1 and R2.

R6 Register, Ramping-down Point

The R6 register is for the ramping-down point used in the varied-speed operation or in-positioning.
If the ramping-down point is set manually or if the number of pulses required for deceleration is set automatically, set R6 to zero or an offset value.

R8 Register, Up/Down Counter

The R8 register allows you to write or read the value of up/down counter for position control.

R9 Register, Environment Setting 1

The R9 register sets logics of input/output pins, operations at signal input and other, 23 particulars in total.

R10 Register, Environment Setting 2

The R10 register sets origin return conditions, the number of output pulses, etc., 9 particulars in total.

R11 Register, Environment Setting 3

The R11 register sets 18 interrupt initiating factors.

R12 Register, Interrupt Factor Monitor

The R12 register allows you to monitor the interrupt signal generating factor which is available in 21 types.

Reading the factor onto the input/output buffer clears the content from the register and cancels the interrupt signal. This register is a read-only register.

R13 Register, Counter Monitor

The read-only register allows you to read four types of data including set pulse rates.

R14 Register, Command Monitor

This read-only register allows you to read applied commands.

R15 Register, Pin Monitor

This read-only register allows you to read the status of 12 pins including $\overline{STA}$ and $\overline{STP}$.

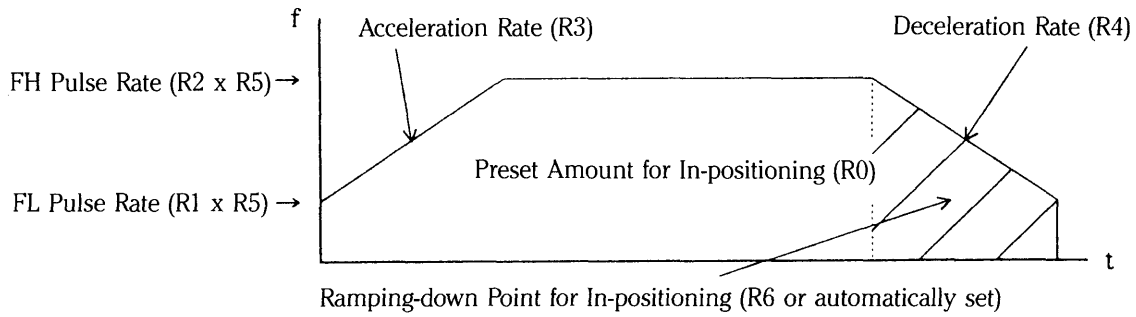
RMD Register, Operation Mode

The RMD register sets 11 operation-related particulars including the operation mode and moving direction.

Other Reading Data

Besides register data, the register read command allows you to read the counting of output pulses for in-positioning and the counting of the ramping-down point used for the automatic deceleration in the varied-speed operation or in-positioning.

Register Data Applied Points on Pulse Output Pattern



3.4 Operation Modes

The PCL5022 provides 9 operation modes, from which a desired one is selected by the RMD register.

3.4.1 Continuous Mode 1

The PCL5022 starts generating pulses upon receiving the start command and continues outputting pulses until receiving the stop command.

3.4.2 Continuous Mode 2

The PCL5022 outputs pulses in synchronization with signals input to PA and PB pins after receiving the start command until receiving the stop command. Use this mode if you wish to drive the motor manually through external pulse input.

3.4.3 Origin Return Mode 1

The PLC5022 stops outputting pulses when conditions for the completion of origin return are satisfied. Conditions for completion of origin return are set in the R10 register (environment setting 2).

3.4.4 Origin Return Mode 2

The PCL5022 stops outputting pulses when it outputs pulses to the number written in the R0 register or when conditions for the completion of origin return are satisfied.

3.4.5 One-pulse Output Mode

The PCL5022 outputs only one pulse irrespective of the number of output pulses entered in the R0 register.

3.4.6 Timer Mode

This mode is to use the internal operation time as a timer. The internal operation is the same as the preset mode 1 below except for no pulse output in this mode.

3.4.7 Preset Mode 1

The PCL5022 puts the axis in position by outputting pulses to the number written in the R0 register.
buffer.

3.4.8 Preset Mode 2

The PCL5022 moves the axis by outputting pulses in synchronization with signals input to PA and PB pins. The number of output pulses is as written in the R0 register.

The PCL5022 output pulses according to input signals to PA and PB pins and stops when outputting pulses to the number written in the R0 register as in the continuous mode 1. The mode is useful for manual in-positioning with external pulse input.

3.4.9 Linear Interpolation Mode

By selecting the linear interpolation mode for the 'a' axis and designating the number of output pulses and the direction for 'a' and 'b' axes, you can let the PCL5022 perform linear interpolation for in-positioning.

3.5 Counters

The PCL5022 provides the preset counter for in-positioning and the ramping-down point counter for automatic deceleration in the varied-speed operation or in-positioning.

3.5.1 Preset Counter

The preset counter is used for in-positioning. When the PCL5022 starts outputting pulses, the preset counter reads the value entered in the R0 register and then it counts down the value at every pulse output. In-positioning is complete when the preset counter counts down to 0. The counting can be read at any time using the register read command.

By writing a specific start command, you can start the PCL5022 without letting the preset counter read the value entered in the R0 register.

The preset counter function is useful to let the PCL5022 output a remaining number of pulses if you stopped it on the way of in-positioning.

3.5.2 Ramping-down Point Counter

The ramping-down point counter is used for automatic start of deceleration in the varied-speed operation or in-positioning. The number of output pulses required for deceleration is calculated at the time of acceleration and the ramping-down point counter is set accordingly. The value is compared with that of the preset counter and when it equals to the latter, deceleration starts while at the same time the ramping-down point counter counts down. You can read the counter value by writing the register read command.

3.6 Control Functions

The PCL5022 provides sophisticated functions to control the motor in various ways.

3.6.1 Microstep Control

Generally, with a microstep stepping motor driver a high in-positioning accuracy is ensured by stopping it at the full step position.

The PCL5022 performs the microstep control to stop microstep motor drivers with a resolution of up to 1/16 at their full step position. For example, if it is set for a microstep of 1/10, the PCL5022 can output 10 times the set number of output pulses.

3.6.2 Out-of-step Detection

The PCL5022 can detect an out-of-step status, provided that the stepping motor has a feedback encoder mounted. When it detects an out-of-step status, the PCL5022 stops outputting pulses.

3.6.3 Idling Pulse Output

The PCL5022 can initiate acceleration after outputting several pulses at the FL rate. This allows you to set the FL rate to a value near the upper limit of self-starting rate of the stepping motor.

3.6.4 Servomotor Interface

The PCL5022 provides the following servomotor control signals:

(1) $\overline{\text{INP}}$

The PCL5022 stops outputting pulses upon receiving this in-position signal, that is, the stop timing is delayed to the input of this signal.

(2) $\overline{\text{ERC}}$

The PCL5022 outputs this one-shot signal to clear the deviation counter of servomotor driver.

(3) $\overline{\text{ALM}}$

The PCL5022 stops outputting pulses upon receiving this alarm signal from the servomotor driver.

3.6.5 Manual Pulser Input

This function allows you to input pulses from the manual pulser to let the PCL5022 output corresponding pulses from $\overline{\text{OUT}}$ and DIR pins for manual operation of a device. From the pulser, the PCL5022 inputs plus and minus pulses or two 90° phase difference signals at PA and PB pins. The 90° phase difference signals can be multiplied.

3.6.6 Up/Down Counter

The up/down counter serves for present position control. It counts output pulses or signals input to EA and EB pins. Signals input to EA and EB pins are plus and minus pulses or 90° phase difference signals. Counted 90° phase difference signals may be multiplied.

3.6.7 Simultaneous Start

With $\overline{\text{STA}}$ pins of multiple units of PCL5022 connected in cascade, you can simultaneously start all units of PCL5022 by writing the start signal to any of $\overline{\text{STA}}$ pins or inputting the start signal through an external circuit.

3.6.8 Simultaneous Stop

With $\overline{\text{STP}}$ pins of multinple units of PCL5022 connected in cascade, you can let the stop signal stop all units of PCL5022 simultaneously. The stop signal may be sent through an external circuit.

3.6.9 Dummy Operation

You can let the PCL5022 perform all activities except for pulse generation. This allows you to check the PCL5022 without running the machine.

3.6.10 External Input Signals from Mechanical System

The PCL5022 can input the following position detecting signals from the mechanical system:

(1) $\overline{+EL}$ and $\overline{-EL}$ Signals

These are limit signals from the mechanical system. The PCL5022 stops outputting pulses immediately upon receiving the limit signal in the moving direction and keeps the stop condition even if the limit signal is turned off.

(2) $\overline{+SD}$ and $\overline{-SD}$ Signals

These are deceleration signals from the mechanical system. The PCL5022 decelerates to the FL rate upon receiving the deceleration signal in the moving direction during varied-speed operation in the continuous or origin return mode. When the deceleration signal is turned off, the PCL5022 accelerates to the FH rate.

(3) $\overline{ORG}$ Signal

This is the origin return signal from the mechanical system. The PCL5022 returns the mechanical system to the origin upon receiving this signal.

3.6.11 Pulse Output Modes

The PCL5022 provides two pulse output modes. The common pulse mode lets it output the control pulse and direction pulse. The 2-pulse mode lets it output plus and minus pulses. You can change the output logic.

3.6.12 Interupt Signal Output

The PCL5022 can output the $\overline{INT}$ signal to the CPU based on any of 21 factors. Interrupt signal generating conditions can be set by the R11 register and the factors can be read from the R12 register. The $\overline{INT}$ signal and the factor are reset by reading the R12 register.

3.7 Monitor

Through designated addresses, you can read kinds of the current status of PCL5022. You can also monitor setting conditions, internal counter values and pin status through registers. Types of status you can monitor through designated addresses are as follows:

3.7.1 Operation Status

You can read the operation status of 'a' or 'b' axis.

3.7.2 AP Pin Status

You can read the status of general-purpose AP pins for 'a' or 'b' axis.

3.7.3 Status of 'a' Axis

You can read the ON/OFF status of $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{EZ}$ and $\overline{ALM}$ signals for 'a' axis.

3.7.4 Status of 'b' Axis

You can read the ON/OFF status of $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{EZ}$ and $\overline{ALM}$ signals for 'b' axis.

3.8 Basic Operation

The basic operation procedure is as follows:

3.8.1 Writing Command

Write command data from the CPU to command addresses.

3.8.2 Reading Status

Read status data from the status address to the CPU.

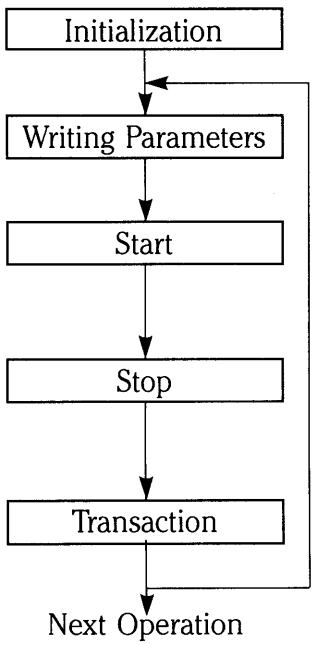
3.8.3 Writing Data to Registers

(1) Write register parameters from the CPU to proper addresses of the input/output buffer.
(2) Write the register write command to transfer register parameters from the input/output buffer to proper registers.

3.8.4 Reading Parameters from Registers

(1) Write the register read command to read the register parameter from the designated register to the input/output buffer.
(2) The CPU will read the register parameter from the address of the input/output buffer.

3.8.5 Typical Operation Procedure



Set the pulse output mode, external input signal logic, interrupt initiating factora, etc.

Write the number of output pulses, pulse rates, operation mode, etc.

Write the start command.

(Read data of position, pulse rate, etc.)

The PCL5022 stops outputting pulses with the stop command, upon completion of preset operation or with an external signal.

Take appropriate transactions such as reading interrupt factors.

4. Software

4.1 Address Map

The address map changes depending on the status of I/$\overline{M}$ pin so that the Intel CPU can access low-place data from a low-place address while the Motorola CPU can access high-place data from a low-place address.

4.1.1 Address Map with I/$\overline{M}$=L, B/$\overline{W}$=L (6809 or the equivalent)

A2	A1	A0	$\overline{US}$	Read Operation	Write Operation
H	H	H	H	Operation status	Operation command buffer
H	H	L	H	AP pin monitor	AP pin output control command buffer
H	L	H	H	'a' axis status	Bit control command buffer
H	L	L	H	'b' axis status	Register control command buffer
L	H	H	H	Input/output buffer Bits 7 to 0	Input/output buffer Bits 7 to 0
L	H	L	H	Input/output buffer Bits 15 to 8	Input/output buffer Bits 15 to 8
L	L	H	H	Input/output buffer Bits 23 to 16	Input/output buffer Bits 23 to 16
L	L	L	H	Input/output buffer Bits 31 to 24	Input/output buffer Bits 31 to 24

4.1.2 Address Map with I/$\overline{M}$=H, B/$\overline{W}$=L (8086 or the equivalent)

	A2	A1	A0	US	Read Operation	Write Operation
Word Access	L	L	L	L	AP pin monitor & operation status	AP output control & operation command
	L	H	L	L	'a' and 'b' axis status	Register control & bit control commands
	H	L	L	L	Input/output buffer Bits 15 to 0	Input/output buffer Bits 15 to 0
	H	H	L	L	Input/output buffer Bits 31 to 16	Input/output buffer Bits 31 to 16
Byte Access	L	L	L	H	Operation status	Operation command buffer
	L	L	H	L	AP pin monitor	AP output control command buffer
	L	H	L	H	'a' axis status	Bit control command buffer
	L	H	H	L	'b' axis status	Register control command buffer
	H	L	L	H	Input/output buffer Bits 7 to 0	Intput/output buffer Bits 7 to 0
	H	L	H	L	Input/output buffer Bits 15 to 8	Input/output buffer Bits 15 to 8
	H	H	L	H	Input/output buffer Bits 23 to 16	Input/output buffer Bits 23 to 16
	H	H	H	L	Input/output buffer Bits 31 to 24	Input/output buffer Bits 31 to 24

4.1.3 Address Map with I/$\overline{M}$=H, B/$\overline{W}$=H (Z80 or the equivalent)

A2	A1	A0	$\overline{US}$	Read Operation	Write Operation
L	L	L	H	Operation status	Operation command buffer
L	L	H	H	AP pin monitor	AP pin output control command buffer
L	H	L	H	'a' axis status	Bit control command buffer
L	H	H	H	'b' axis status	Register control command buffer
H	L	L	H	Input/output buffer Bits 7 to 0	Input/output buffer Bits 7 to 0
H	L	H	H	Input/output buffer Bits 15 to 8	Input/output buffer Bits 15 to 8
H	H	L	H	Input/output buffer Bits 23 to 16	Input/output buffer Bits 23 to 16
H	H	H	H	Input/output buffer Bits 31 to 24	Input/output buffer Bits 31 to 24

4.2 Word Access

If you use the 16-bit data bus, you can write a word into the command buffer, AP output control command buffer, bit control command buffer and register control command buffer.

NOTE: If you try to read through byte access with 16-bit data bus connected, the bits of data bus which are not selected are put at high impedance.

4.3 Read/Write from/to Registers

In the following description, addresses are of the interface for the Z80.

4.3.1 Writing Procedure

(1) Write data in the input/output buffer in a desired order.

(2) Write one of register write commands (40HEX to 4FHEX, C0HEX to CFHEX, 7FHEX, FFHEX) to the address (No. 3) of register control command.

Precaution: To permit internal processing, do not write data or command for a time length of four cycles at the reference clock (approximately 0.4μs with a reference clock of 9.8304MHz).

4.3.2 Reading Procedure

(1) Write one of register read commands (00HEX to 0FHEX, 80HEX to 8FHEX, 3CHEX, 3DHEX, 3FHEX, BCHEX, BDHEX, BFHEX) to the address (No. 3) of register control command.

(2) To permit internal processing, wait for a time length of four cycles at the reference clock (approximately 0.4μs with a reference clock of 9.8304MHz).

(3) Read data from the input/output buffer in a desired order.

NOTE: If the PCL5022 is interfaced with the CPU via the $\overline{WRQ}$ pin, the abovementioned waiting step is automatically processed.

4.4 Reading Status

Since the status at the start of processing for reading is latched, the data bus does not change during a read cycle. But if you want to continuously read the status, allow a time length of four cycles at the reference clock. If it is not secured, the previous data may be read out. If the PCL5022 is interfaced with the CPU via the $\overline{WRQ}$ pin, the time interval is automatically processed.

You can monitor the present operation status, interrupt request, the status of general-purpose input/output pins (AP0 to AP3) and ON/OFF conditions of $\overline{\pm EL}$, $\overline{\pm SD}$ (with latch), $\overline{ORG}$ (with latch), $\overline{EZ}$ and $\overline{ALM}$ pins for each axis. You can also monitor $\overline{\pm SD}$ (through), $\overline{\pm ORG}$ (through), $\overline{INT}$, $\overline{ERC}$, $\overline{INP}$, $\overline{CLR}$, $\overline{BSY}$, $\overline{FUP}$, $\overline{FDW}$, $\overline{STA}$ and $\overline{STP}$ signals through the R15 register.

4.5 Default Conditions

Items	Default (Reset) Conditions
All internal registers	0
Operation command buffer	00_{HEX}
AP output control command buffer	00_{HEX}
Bit control command buffer	00_{HEX}
Register control command buffer	00_{HEX}
Input/output buffer	00000000_{HEX}
$\overline{INT}$ pin	High level
Pins D0 to D7	High impedance
Pins D8 to D15	High impedance
Pins AP0 to AP3	High level
$\overline{OUT}$ pin	High level
DIR pin	High level
$\overline{ERC}$ pin	High level
$\overline{WRQ}$ pin	High level
$\overline{BSY}$ pin	High level
$\overline{FUP}$ pin	High level
$\overline{FDW}$ pin	High level

4.6 Precautions in Designing Software

If you connect the PCL5022 to the CPU without using the $\overline{WRQ}$ output signal, allow a time length of four cycles at the reference clock:

1) From writing a register read command into the register control command address (No. 3) to reading the data.
2) From writing a register write command into the register control command adress (No. 3) to writing the next data
3) From writing a command (except for an AP output control command) to writing the next command.

Be sure to set registers R1 to R5 at a value other than 0 and set the register R2 at a value higher than R1.

5. Operation

5.1 Setting Pulse Output Pattern

5.1.1 Setting Pulse Output Pattern with Acceleration and Deceleration

You can let the PCL5022 output pulses with acceleration at the start and deceleration at the end. Set registers R1 to R5 at desired parameters. If the parameters may be the same as previous, you need not write anew. When these parameters are read as 32-bit data, unused high-place bits are all 0.

R1: FL Rate Register, 14 bits

Write the FL pulse rate in this register in a range of 1 to 16,383 (3FFF$_{HEX}$). The rate is multiplied by the parameter written in the R5 register to be used for the constant speed operation at the FL rate or at the start/stop of varied-speed operation.

FL pulse rate (pps) = (R1 parameter) x (R5 parameter)

R2: FH Pulse Rate Register, 14 bits

Write the FH pulse rate in this register in a range of 1 to 16,383 (3FFF$_{HEX}$). The rate should be higher than what is written in the R1 register. The rate is multiplied by the parameter written in the R5 register to be used for the constant-speed operation at the FH pule rate or for the high-speed operation in the varied speed mode.

FH pulse rate (pps) = (R2 parameter) x (R5 parameter)

R3: Acceleration Parameter Register, 14 bits

Write the acceleration parameter for the varied-speed operation in this register. The setting range is 1 to 16,383 (3FFF$_{HEX}$). If the ramping-down point is automatically set, the R3 parameter is used for deceleration. Relations between the R3 parameter and acceleration/deceleration time are as follows:

$$\text{Accel/decel time (sec)} = \frac{[(R2) - (R1)] \times (R3 + 1) \times 4}{\text{Reference clock (Hz)}}$$

R4: Deceleration Parameter Register, 14 bits

Write the deceleration parameter for the varied-speed operation in this register. The setting range is 1 to 16,383 (3FFF$_{HEX}$). The parameter has the function if the ramping-down point is manually set by setting bit 8 of RMD register at 1. Relations between the R4 parameter and deceleration time are the same as those between the R3 parameter and acceleration time.

R5: Multiplication Factor Register, 12 bits

Write a multiplication factor in this register in a range of 1 to 4096 (FFF$_{HEX}$). R1 and R2 parameters are multiplied by the factor. The higher the multiplication factor, the coarser the pulse rate setting interval becomes. Usually, therefore, a smaller multiplication factor is used. Relations between a set value and multiplication factor are as follows:

$$\text{Multiplication factor} = \frac{\text{Reference clock (Hz)}}{(R5 + 1) \times 65536}$$

Examples with a reference clock of 9.8304MHz (Output pulse rate in pps)

Set Value	Multiplication	Output Pulse Rate	Set Value	Multiplication	Output Pulse Rate
2999 (0BB7HEX)	0.05	0.05 to 819.15	49 (31HEX)	3	3 to 49149
1499 (5DBHEX)	0.1	0.1 to 1638.3	29 (1DHEX)	5	5 to 81915
749 (2EDHEX)	0.2	0.2 to 3276.6	14 (0EHEX)	10	10 to 163830
299 (12BHEX)	0.5	0.5 to 8191.5	4 (4HEX)	30	30 to 491490
149 (95HEX)	1	1 to 16383	2 (2HEX)	50	50 to 819150
74 (4AHEX)	2	2 to 32766	1 (1HEX)	75	75 to 1228725

5.1.2 Typical Pulse Output with Acceleration/Deceleration

To set a starting pulse rate at 10 pps, an operating pulse rate at 50 kpps and an acceleration time at 300ms with the reference clock of 9.8304MHz:

(1) Supposing the 5x mode is used for the operating pulse rate of 50 kpps, write 29 (1DHEX) into the R4 register.

(2) To obtain the starting pulse rate of 10 pps in the 5x mode, write 2 (0002HEX) into the R1 register.

(3) To obtain the operating pulse rate of 50 kpps in the 5x mode, write 10000 (2710HEX) into the R2 register.

(4) Calculate the parameter to be written in the R3 register for the acceleration time of 300ms.

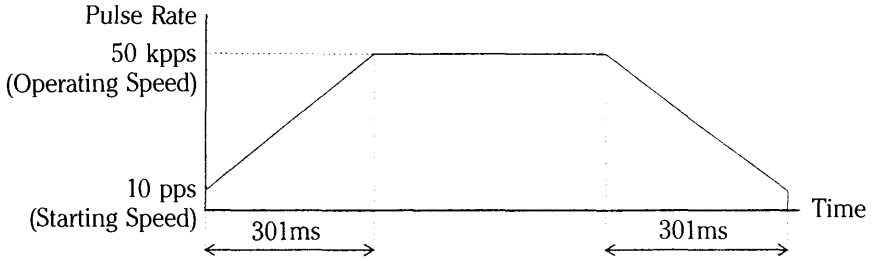
$$\text{Acceleration time (sec)} = \frac{[(R2) - (R1)] \times (R3 + 1) \times 4}{\text{Reference clock (Hz)}}$$

$$0.3 \text{ (sec)} = \frac{(10000 - 2) \times (R3 + 1) \times 4}{9{,}830{,}400 \text{ (Hz)}}$$

Thus, R3 parameter = 72,743

However, since the parameter you can write into the R3 register is an integer, write 72 or 73 into the R3 register.

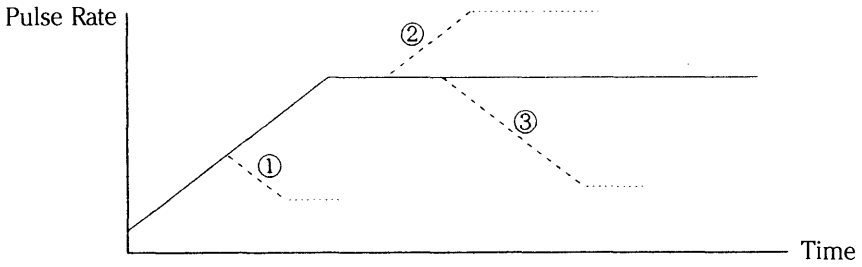
The pulse output pattern with R3=73 is as follows:



5.1.3 Changing Pulse Output Pattern during Operation

You can change the pulse output pattern during operation by rewriting parameters to R2, R3 and R4 registers. However, if you set bit 8 of RMD register at 0 for automatic ramping-down point selection in the origin return mode 2, preset mode 1 or linear interpolation mode, do not change the R3 parameter during operation. The automatic setting function cannot follow the change during operation.

Typical Pulse Output Pattern Changed during Operation



① If you change R2 parameter to a lower rate during acceleration, pulse output decelerates to the new FH rate in a symmetrical pattern.

② ③ If you change R2 parameter after acceleration, pulse output accelerates or decelerate to the new FH rate.

5.1.4 Setting Ramping-down Point

It may be required to let the PCL5022 ramp down the pulse output before stopping in-positioning operation in the preset mode 1, origin return mode 2 or linear interpolation mode. If you select the automatic ramping-down point setting function, the internal ramping-down point counter counts the number of pulses required for acceleration and lets the PCL5022 use the counting as the starting point of deceleration.

R6: Ramping-down Point Register, 24 bits

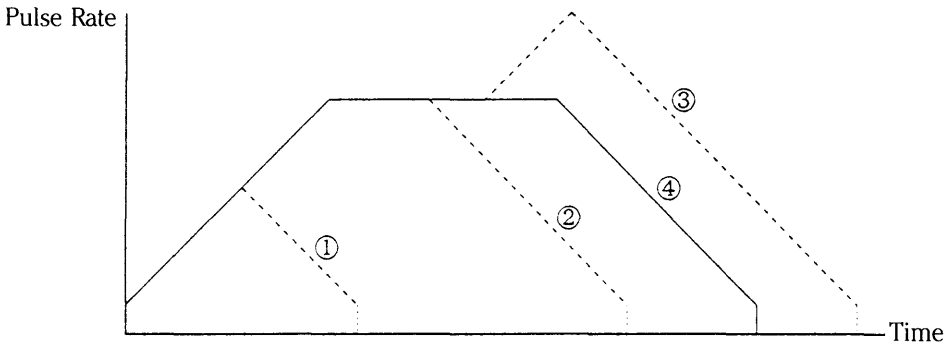
The ramping-down point is used for the varied-speed operation in the preset mode (in-positioning). Write the ramping-down point in this register in a range of 0 to 4,194,303 (3FFFFF$_{HEX}$).

The effect of set R6 parameter differs depending on setting of the RMD register as follows:

- If bit 8 of RMD register is set at 0 (automatic);
  Write a signed parameter in the R6 register, which is offset from the automatic setting. A positive value lets the PCL5022 start deceleration earlier and output pulses at the FL rate after deceleration. A negative value starts the PCL5022 delay the start of deceleration. If any offset is required, write 0 in the R6 register. The setting range is −2,097,152 (200000$_{HEX}$) to +2,097,151 (1FFFFF$_{HEX}$).
- If bit 8 of RMD register is set at 1 (manual):
  Write the number of pulses in the R6 register. The PCL5022 will start deceleration at that number of pulses before stop. That is, deceleration starts with a timing of (preset counter) ≦ (R6 parameter).

$$\text{R6 parameter (number of pulses)} = \frac{[(R2)^2 - (R1)^2] \times (R4 + 1)}{(R5 + 1) \times 32{,}768}$$

Pulse Output Pattern Varied with Ramping-down Points



① If the ramping-down point comes during acceleration, the PCL5022 decelerates the pulse output to the FL pulse rate in a symmetrical pattern to the acceleration made until then.

② If the ramping-down point comes during deceleration initiated by switch-over of pulse rate, the PCL5022 continues decelerating the pulse output to the FL rate. (Switchover of pulse rate compensates the ramping-down point by deceleration in negative direction.)

③ If the ramping-down point comes during acceleration initiated by switch-over of pulse rate, the PCL5022 decelerates the pulse output to the FL rate. (Switchover of pulse rate compensates the ramping-down point by acceleration in positive direction.)

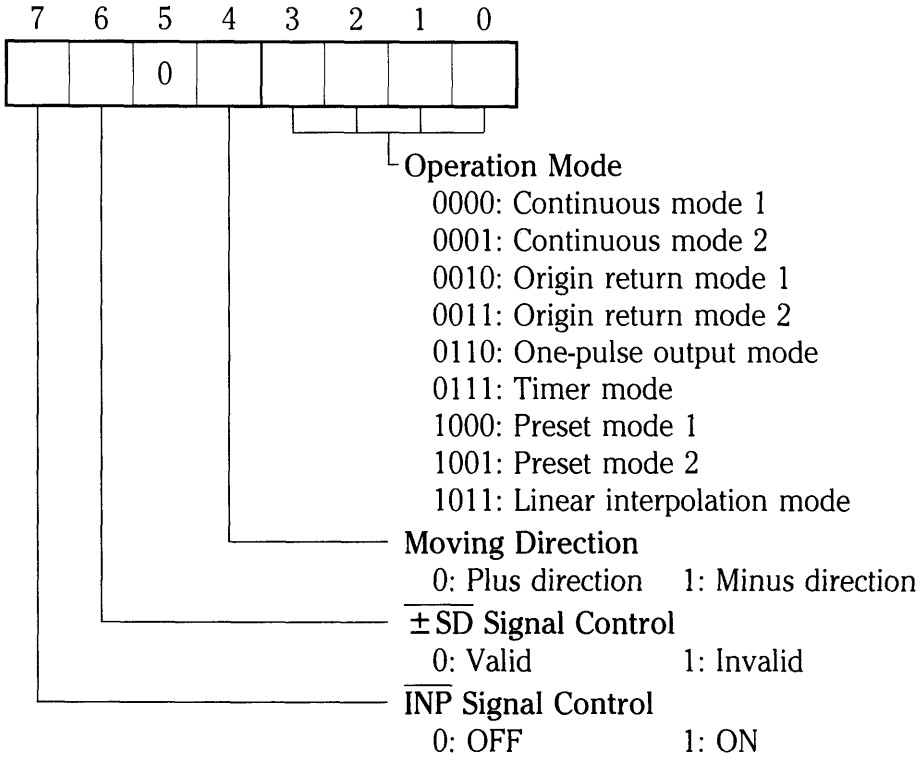
④ If the ramping-down point comes after acceleration/deceleration, the PCL5022 decelerates the pulse output to the FL rate.

• A deceleration pattern changed by writing the deceleration command (02, 82, 42HEX) or deceleration stop command (0A, 8A, 4AHEX) to the operation command address (No. 0) or with the ± SD signal input is the same as above.

5.2 Operation Mode Register

The operation mode register (RMD registeer) provided for each axis allows you to write a desired operation mode and operating conditions via the input/output buffer.

5.2.1 Operation Mode Register (RMD Register)



(1) Operation Mode

Enter the 4-digit code to select a desired operation mode from nine. Selection of the linear interporation mode is available for 'a' axis only. If you select it for 'b' axis, it has no function. Also, be sure to enter one of codes listed above. If you enter a different code, normal operation is not guaranteed.

(2) Moving Direction

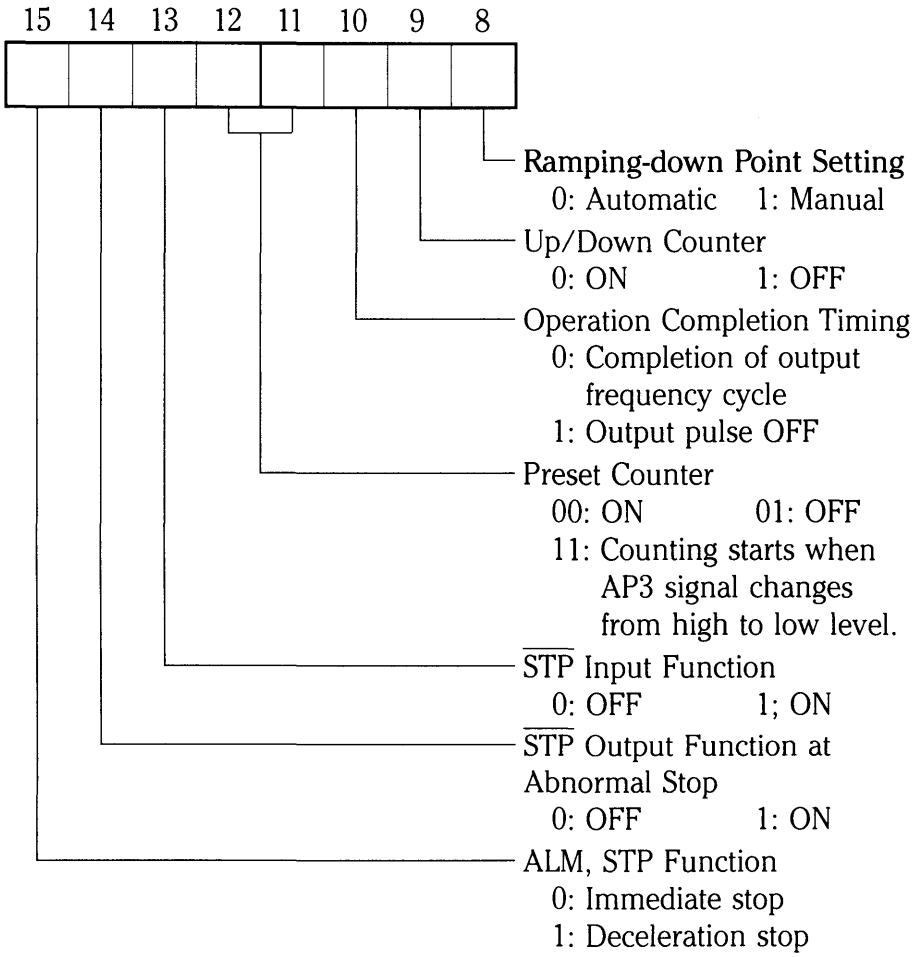
Designate a desired moving direction by entering 0 or 1. Note, however, that the moving direction designated here is neglected in the continuous mode 2. With the plus direction selected, the up/down counter counts up.

(3) $\overline{\pm SD}$ Signal Control

Select whether or not to make the input to $\overline{+SD}$ and $\overline{-SD}$ pins valid. If this bit is set at 0, deceleration is made to the FL pulse rate when an $\overline{SD}$ signal in the moving direction is input during varied-speed operation. If the bit is set at 1, any $\overline{SD}$ signal is masked and does not cause deceleration. The setting condition of this bit has no relation with the $\overline{SD}$ input status on monitor.

(4) INP Signal Control

The servomotor operates with a delay to command pulses. So, it does not stop immediately when the PCL5022 completes outputting pulses. The PCL5022, therefore, inputs the motor stop signal (in-position signal) from the motor driver through the $\overline{INP}$ pin. If the bit is set at 1, the operation completion timing delays to the time point when the $\overline{INP}$ pin is turned on. Operation status, $\overline{BSY}$ and $\overline{INT}$ signals are also delayed.



(5) Ramping-down Point Setting Method

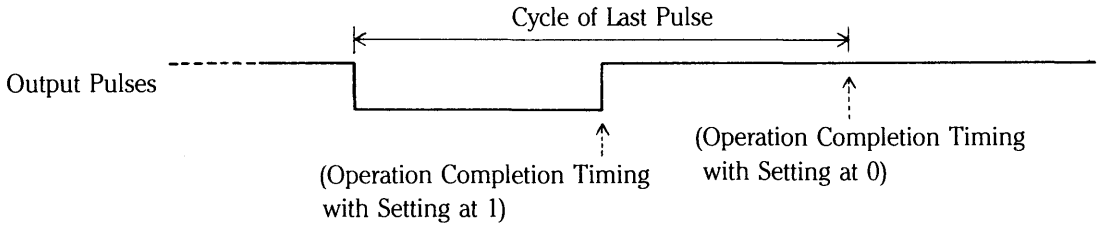
With the preset mode, linear interpolation mode or origin return mode 2 selected, the PCL5022 ramps down the pulse output when the preset counter value becomes equal or lower than the ramping-down point. Bit 8 allows you to select the ramping-down point setting method, automatic or manual. If you select the automatic method, the R6 parameter will be offset and the ramping-down point will be a sum of the number of pulses required for acceleration and the R6 parameter. If you select the manual method, the R6 parameter is the ramping-down point.

(6) Up/Down Counter

If this bit is set at 1, the up/down counter stops operating. Set it at 1 when you need to operate without activating the up/down counter for the purpose of correcting backlash, etc. For your reference, the up/down counter does not count or in timer mode operation if the bit is set at 0.

(7) Operation Completion Timing

You can select a timing the PCL5022 stops outputting pulses. Set the bit at 0. The PCL5022 will stop outputting pulses when a cycle at the output pulse rate will be complete. Thus, you can secure a pause time if you restart immediately after stopping. Set the bit at 1. The PCL5022 will stop outputting pulses when an output pulse is off. Since the PCL5022 stops without waiting for completion of the cycle, you can shorten the cycle time if you do not restart immediately after stopping. Set it at 0 if the linear interpolation mode is selected.



(8) Preset Counter

Set these bits at 01. The preset counter will stop counting down. Accordingly, if you operate the PCL5022 in the preset mode with these bits set at 01, the PCL5022 operates in a similar mode to the continuous mode and it will stop upon outputting pulses to the preset number from the time point when these bits are newly set at 00. If you set these bits at 11, the PCL5022 operates like in the continuous mode and will stop upon outputting pulses to the preset number from the time point when the AP3 signal changes from high to low level, at the edge of which the preset counter starts counting. Set these bits at 00 if the linear interpolation mode is selected.

(9) $\overline{\text{STP}}$ Input Function

For simultaneous stop of multiple axes, $\overline{\text{STP}}$ pins of all PCL5022 should be connected in cascade. By setting this bit at 0, you can place the pin in an unconnected condition.

(10) $\overline{\text{STP}}$ Output Function at Abnormal Stop

By setting this bit, you can let the PCL5022 output the STP signal when the $\overline{\pm\text{EL}}$ stops the PCL5022 from outputting pulses or the $\overline{\text{ALM}}$ or $\overline{\pm\text{SD}}$ signal lets the PCL5022 decelerates and then stop outputting pulses or when an out-of-step status is detected.

(11) $\overline{\text{ALM}}$, $\overline{\text{STP}}$ Stop Method

This bit allows you select how the $\overline{\text{ALM}}$ and $\overline{\text{STP}}$ signals stop the PCL5022 from outputting pulses. Set the bit at 1. The $\overline{\text{ALM}}$ or $\overline{\text{STP}}$ signal will let the PCL5022 stop outputting pulses after deceleration. Note, however, that these signals immediately stop the PCL5022 which is operating in the constant-speed mode at the FL pulse rate.

Typical Settings vs. Operation Modes (Bits 7 to 0)

Settings									Operation Modes
7	6	5	4	3	2	1	0	HEX	
0	0	0	0	0	0	0	0	00	Continuous mode 1 in plus direction
0	0	0	1	0	0	0	0	10	Continuous mode 1 in minus direction
0	0	0	0	0	0	0	1	01	Continuous mode 2
0	0	0	0	0	0	1	0	02	Origin return mode 1 in plus direction
0	0	0	1	0	0	1	0	12	Origin return mode 1 in minus direction
0	0	0	0	0	0	1	1	03	Origin return mode 2 in plus direction
0	0	0	1	0	0	1	1	13	Origin return mode 2 in minus direction
0	0	0	0	0	1	1	0	06	One-pulse output mode in plus direction
0	0	0	1	0	1	1	0	16	One-pulse output mode in minus direction
0	0	0	0	0	1	1	1	07	Timer mode
0	0	0	0	1	0	0	0	08	Preset mode 1 in plus direction
0	0	0	1	1	0	0	0	18	Preset mode 1 in minus direction
0	0	0	0	1	0	0	1	09	Preset mode 2 in plus direction
0	0	0	1	1	0	0	1	19	Preset mode 2 in minus direction
0	0	0	0	1	0	1	1	0C	Linear interpolation mode ('a' axis, plus)
0	0	0	1	x	x	x	x	1n	Linear interpolation mode ('b' axis, minus)
n	0	0	n	n	n	n	n	——	$\overline{\pm\text{SD}}$ signal validin minus direction
n	1	0	n	n	n	n	n	——	$\overline{\pm\text{SD}}$ signal invalid
0	n	0	n	n	n	n	n	——	$\overline{\text{INP}}$ signal control OFF
1	n	0	n	n	n	n	n	——	$\overline{\text{INP}}$ signal control ON

(Bits 15 to 8)

Settings								Operation Modes
7	6	5	4	3	2	1	0	
n	n	n	n	n	n	n	0	Ramping-down point setting method (auto)
n	n	n	n	n	n	n	1	Ramping-down point setting method (manual)
n	n	n	n	n	n	1	n	Up/down counter ON
n	n	n	n	n	n	1	n	Up/Down counter OFF
n	n	n	n	n	0	n	n	Operation completion timing: Cycle
n	n	n	n	n	1	n	n	Operation completion timing: Pulse OFF
n	n	n	0	0	n	n	n	Preset counter ON
n	n	n	0	1	n	n	n	Preset counter OFF
n	n	n	1	1	n	n	n	Preset counter starts with AP3 H to L
n	n	0	n	n	n	n	n	$\overline{\text{STP}}$ input function OFF
n	n	1	n	n	n	n	n	$\overline{\text{STP}}$ input function ON
n	0	n	n	n	n	n	n	$\overline{\text{STP}}$ output function OFF
n	1	n	n	n	n	n	n	STP output function ON
0	n	n	n	n	n	n	n	$\overline{\text{ALM}}$, $\overline{\text{STP}}$: Immediate stop
1	n	n	n	n	n	n	n	$\overline{\text{ALM}}$, $\overline{\text{STP}}$: Stop after deceleration

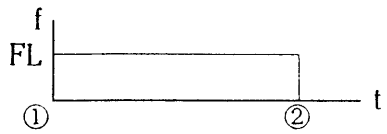
n: Depends on other setting. x: Invalid

5.3 Operation Modes

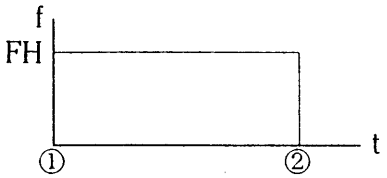
In any operation mode an $\overline{EL}$ signal in the moving direction stops the PCL5022 from outputting pulses. In varied-speed operation an $\overline{SD}$ signal in the moving direction lets the PCL5022 decelerate or stop pulse output after deceleration.

5.3.1 Continuous Mode 1

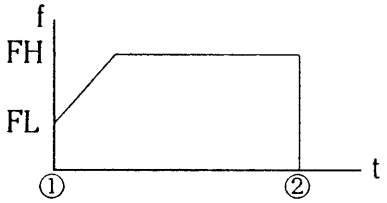
In this mode, writing the start command lets the PCL5022 output pulses in the direction set by bit 4 of the operation mode register until the stop command is written.



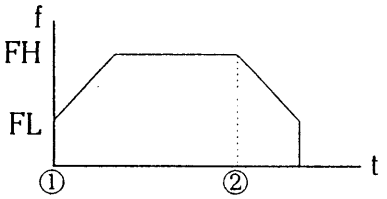
① Writing start command for constant speed operation at FL pulse rate
② Writing immediate stop command



① Writing start command for constant-speed operation at FH pulse rate
② Writing immediate stop command



① Writing start command for varied-speed operation
② Writing immediate stop command

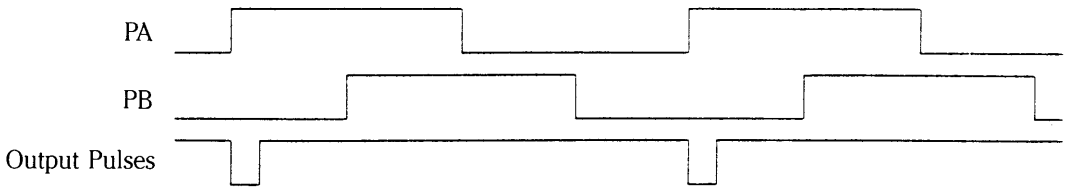


① Writing start command for varied-speed operation
② Writing deceleration stop command

5.3.2 Continuous Mode 2

In this mode, external pulse signals to PA and PB pins let the PCL5022 operate like in the continuous mode 1. For operation in this mode, you need to use the start command for varied-speed operation. You can control the number of output pulses and the pulse rate based on input PA and PB signals but the upper limit of pulse rate is the set FH pulse rate. The moving direction depends on PA and PB signals and the status of bit 4 of operation mode buffer is invalid. For details, refer to 5.4.5 Manual Pulser Input."

Pulse output with 1x 90° phase difference signals input to PA and PB pins



5.3.3 Origin Return Mode 1

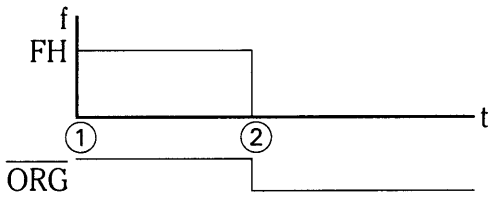
In this mode you can let the PCL5022 output pulses until the condition to complete the origin return is satisfied after writing the start command. The moving direction is as set by bit 4 of the RMD register. If you set bit 6 of R10 register (environment setting 2) at 1 in advance, the up/down counter will be reset upon completion of the origin return.

Select a condition to complete the origin return by setting bits 5–0 of R10 as follows. (Refer to 5.4.10 External Input Signals from Mechanical System, $\overline{\text{ORG}}$ Signal.)

(1) 00xxxx (bits 5 to 0 of R10)

The $\overline{\text{ORG}}$ signal stops the PCL5022 from outputting pulses. If the signal is on at the start, the PCL5022 outputs no pulse and completes the operation. (Bits 3–0 have no concern with this mode.)

In the case of setting 00xxxx

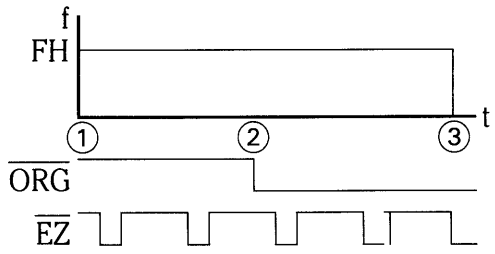


① Writing start command for constant-speed operation at FH pulse rate
② $\overline{\text{ORG}}$ signal ON

(2) 01nnnn (bits 5 to 0 of R10)

The (nnnn +1)th $\overline{\text{EZ}}$ signal after the $\overline{\text{ORG}}$ signal ON stops the PCL5022 from outputting pulses. To effect the origin return, the $\overline{\text{ORG}}$ signal should be ON or latched during the time EZ signals are input in that number.$\overline{\text{ORG}}$ If the $\overline{\text{ORG}}$ signal is ON at the start, the PCL5022 stops outputting pulses after the $\overline{\text{EL}}$ signals are counted to that number anew.

In the case of setting "010010"

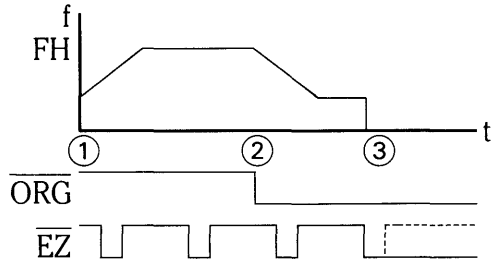


① Writing start command for constant-speed operation at FH pulse rate
② $\overline{\text{ORG}}$ signal ON
③ The 3rd $\overline{\text{EZ}}$ signal ON

(3) 10nnnn (bits 5 to 0 of R10)

The $\overline{\text{ORG}}$ signal which is turned on during varied-speed operation initiates deceleration and the (nnnn +1)th $\overline{\text{EZ}}$ stops the PCL5022 from outputting pulses. To effect the origin return, the $\overline{\text{ORG}}$ signal should be ON or latched during the time EZ signals are input in that number. If the $\overline{\text{ORG}}$ signal If the $\overline{\text{ORG}}$ signal is ON at the start, the PCL5022 stops outputting pulses after the $\overline{\text{EL}}$ signals are counted to that number anew. The constant-speed operation shows the same effect as setting 01nnnn.

In the case of setting "100001"



① Writing start command for varied-speed operation
② $\overline{\text{ORG}}$ signal ON
③ The 2rd $\overline{\text{EZ}}$ signal ON

You can change the input logic of $\overline{\text{ORG}}$ signal with bit 5 of R9 register, and that of the EZ signal with bit 7 of R9 register.

5.3.4 Origin Return Mode 2

In this mode you can let the PCL5022 output pulses until the axis returns to the origin or pulses are output in a preset number. When started, the PCL5022 outputs pulses like in the origin return mode 1 but if the number of output pulses reaches the preset R0 register value before the origin return, it stops outputting pulses. Set the moving direction with bit 4 of the RMD register. You can know the cause of stop, origin return or pulses output in a preset number, by reading the R12 register or preset counter value. Based on the preset counter value, you can know that pulses output in a preset number stopped the PCL5022 if the counter value is 0 and the origin return stopped the PCL5022 if the counter value is other than 0. If you want to judge the cause through the R12 register, set bits 5 and 6 of R11 at 1 in advance and judge the cause of stop with bit 11 (pulses output to a preset number) and bit 9 (origin return) of R12.

5.3.5 One-pulse Output Mode

In this mode you can let the PCL5022 output only one pulse (or pulses in a unit number if the microstep control is used). Set the moving direction with bit 4 of the RMD register. Operation in this mode is the same as in the preset mode 1. But you need not write 1 in the R0 register. The preset counter counts down referring to 1.

5.3.6 Timer Mode

This mode allows you to use the PCL5022 as a timer referring to internal operation time with no pulse output. The preset counter counts down referring to the R0 parameter. $\overline{\text{EL}}$ and $\overline{\text{SD}}$ signals are invalid (always regarded as OFF). In the timer mode, the up/down counter stops counting. If the direction signal is output from the DIR pin in the common pulse mode, the status of DIR pin changes according to bit 4 of the operation mode register. To start the time mode, use the start command for constant-speed operation. The internal operation time is the product of a cycle of output pulses and the R0 register value (e.g. 1000 pps x 120 pulses (R0 register value) = 120ms). Irrespective of the status of bit 7 of the RMD register, the INP signal does not delay the completion of operation.

5.3.7 Preset Mode 1

In this mode you can place the axis in a desired position by designating the number of pulses and the direction. Write the number of output pulses in the R0 register and the moving direction in bit 4 of the operation mode register. The setting range for the R0 register is 0 to 268,435,445.

5.3.8 Preset Mode 2

In this mode you can place the axis in synchronization with signals input to PA and PB pins. Write the number of pulses in the R0 register and the moving direction with bit 4 of the operation mode register. The PCL5022 outputs pulses line in the continuous mode 2 based on PA and PB input. However, the moving direction is as set with bit 4 of the RMD register and has no relation with PA and PB input. For details, refer to "5.4.5 Manual Pulser Input."

5.3.9 Linear Interpolation Mode

You can let the PCL5022 put two axes in linear interpolation position by designating the number of pulses and the direction for each of 'a' and 'b' axes and placing the 'a' axis in the linear interpolation mode. (Until the 'a' axis is placed in other than the linear interpolation mode, the mode setting for the 'b' axis has no function.)

The axis which is set at a higher number of pulses is the main axis (if both axes are set at the same number of pulses, the 'a' axis is the main axis). Pulse rates (R1 and R2), acceleration/deceleration rates (R3 and R4), multiplication factor (R5), unit number of output pulses (R10), ramping-down point setting method and simultaneous stop method (RMD) written for the main axis are used. The start/stop commands which are written to the 'a' axis are used. Define the completion of preset operation of both 'a' and 'b' axes as an interrupt factor by setting bits 6 and 7 of the R11 register of 'a' axis at 1.

Relations between speeds of main and slave axes are as follows:

$$\text{Speed of slave axis} = \text{Speed of main axis} \times \frac{\text{Set pulse rate of slave axis}}{\text{Set pulse rate of main axis}}$$

Composite speed of both axes with 'a' axis put orthogonal to 'b' axis is as follows:

$$\text{Composite speed} = \text{Speed of main axis} \times \frac{\sqrt{(\text{Set number of pulses for main axis})^2 + (\text{Set number of pulses for slave axis})^2}}{\text{Set number of pulses for main axis}}$$

$$\text{or} = \text{Speed of main axis} \times \sqrt{1 + \left(\frac{\text{Set number of pulses for slave axis}}{\text{Set number of pulses for main axis}}\right)^2}$$

Precautions in Operating in Linear Interpolation Mode

- If the preset moving amount (R0) for either 'a' or 'b' axis is set at 0, do not use the linear interpolation mode but use the preset mode 1.
- The value of speed monitor (R13) of 'a' axis is that of main axis. The speed of slave axis cannot be monitored. (The speed monitor (R13) of 'b' axis is fixed to the FL pulse rate (R1) of 'b' axis.)
- Acceleration/deceleration timing by idling pulses or a ramping-down point is a logical sum of 'a' and 'b' axes. (When idling pulses are being output with either 'a' or 'b' axis, operation is at at the FL pulse rate. When either 'a' or 'b' axis comes to the ramping-down point, deceleration starts.)
- Operation completion timing of the RMD (operation mode) register and the preset counter operation should not be set at other than 0.

5.4 Control Functions

5.4.1 Microstep Control

You can perform microstep control to suppress the step vibration of stepping motor. Use of a microstep driver may suppress the step vibration but the positioning accuracy is not ensured unless it stops at a full-step position. The PCL5022 has a function to stop the motor at a full-step position. Furthermore, the R0 register (preset amount) and the up/down counter (R8) use the number of full steps irrespective of the microstep control.

Resolution of microstep is $1/n$ (n is available in a range of 1 to 16). Set the "unit number of output pulses" of R10 register7 at (n − 1) to determine a resolution. If it is set at 0, the resolution is 1/1 (= full step). The output frequency is the same as in the case the microstep control is not used. If the PCL5022 is operated in the preset mode with the resolution set at 1/10 (set value = 9) and R0 set at 12, the PCL5022 outputs 120 pulses to change the present position by 12 counts.

Under the microstep control, the PCL5022 stops after outputting pulses in the unit number and does not stop on the way. However, the emergency stop command or $\overline{\text{RST}}$ signal stops the PCL5022 at other than full-step position. Also, by writing a microstep control range, you can let the $\overline{\pm\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or completion of origin return stop the PCL5022 immediately in other than full-step position. Such the operation is useful to control the motor in some number of units and not for the purpose of microstep. (e.g. to control the machine which moves by 0.2μm per pulse, in a unit of 1μm)

- To set the unit number of output pulses for the microstep control
  Write a value of (resolution of microstep − 1) in bits 19 to 16 of R10. The setting range is 0 to 15.
- To set the microstep control range
  Set bit 12 of R10 at—
  0: Microstep control at all times
  1: No microstep control at the stop initiated by the $\overline{\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or completion of origin return.
- Emergency stop command (bit control command)
  Write the command during operation in progress. The PCL5022 will immediately stop even in other than full-step position.
  Bit control command (HEX)

'a' axis	'b' axis	a/b
2B	BA	6B

5.4.2 Out-of-step Detection

The PCL5022 is equipped with a 6-bit deviation counter with (±) signs to detect an out-of-step status of stepping motor. Mount a feedback encoder onto the stepping motor. The deviation counter will count a deviation between command pulses and pulses fed back from the encoder and if the value exceeds a certain level (1 to 31), the PCL5022 will judge an out-of-step status and stop generating pulses while outputting the $\overline{INT}$ signal. The encoder should have the same resolution as the stepping motor (or a resolution of full step under the microstep control).

This detection function is effective whether the motor is operating or not. So you can detect a deviation due to an external force applied during suspension. Set bits R11 at a maximum deviation which will be compared with the deviation counter value. If you set at 00000 (default), the out-of-step detection function is deactivated.

The encoder mounted onto the stepping motor feeds back plus and minus pulses or 90° phase difference signals to ERA and ERB pins. 90° phase difference signals multiplied by 1, 2 or 4 may be counted. A simultaneous change of ERA and ERB input status causes an error, thereby letting the PCL5022 output the $\overline{INT}$ signal.

You can read the value of the deviation counter for out-of-step detection throuh the R13 register and reset it by writing the deviation counter clear command.

- Deviation counter value for out-of-step detection
  Write a maximum deviation value in bits 12 to 8 of R11. The setting range is 0 to 31. When the PCL5022 detects an out-of-step status, it immediately stops outputting pulses while outputting the $\overline{INT}$ signal.
- Read bit 6 of R12. If the interrupt factor is out-of-step detection, the bit is 1.
- To let ERA/ERB input error initiate the $\overline{INT}$ signal output, set bit 14 of R11 at 1. The $\overline{INT}$ signal will be when both ERA and ERB (EA, EB - PA, PB) inputs change simultaneously.
- Read bit 13 of R12. If it is 1, the interrupt factor is ERA, ERB input error.
- To select ERA, ERB input mode, set bits 15 and 14 of R9 at—
  00: 1x 90° phase difference signal
  01: 2x 90° phase difference signal
  10: 4x 90° phase difference signal
  11: Up/down 2 pulse input
- Deviation counter value (bits 31 to 24 of R13)
  The value of 6-bit deviation counter with a sign is read in 8 bits by extension for the sign. A negative value is a twos compement and a positive value is when the motor is in a minus position from the integrated position.

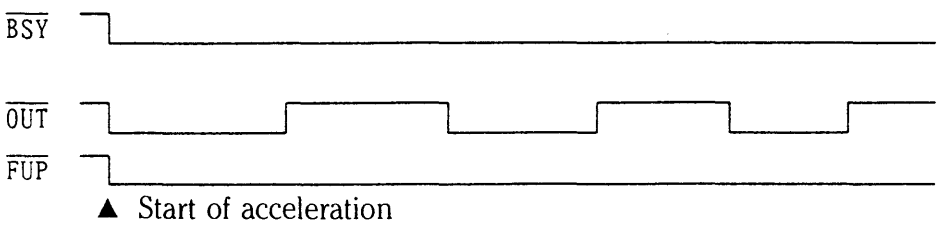
- Deviation counter clear command (bit control command)
  Bit control command (HEX)

'a' axis	'b' axis	a/b
0A	8A	4A

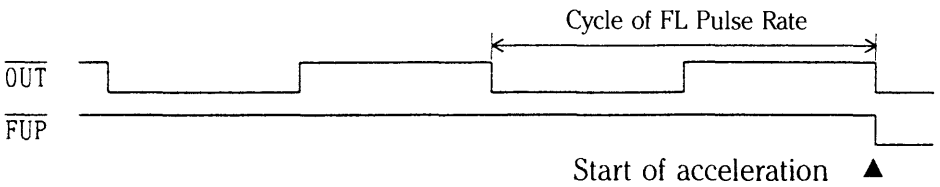
5.4.3 Idling Pulse Output

Usually, in the varied-speed operation the PCL5022 starts acceleration upon outputting the first pulse. Using the idling pulse output function, you can let the PCL5022 initiate acceleration after outputting several pulses at the FL pulse rate. If you do not use this function, the first pulse cycle is shorter than that of the set FL pulse rate because acceleration starts upon output of the first pulse. Due to this, the pulse rate at the start of accleration is higher than the set FL pulse rate. If you use the idling pulse output function, the timing to initiate acceleration is delayed by the set number of idling pulses, thereby making the initial rate the FL pulse rate and allowing you to set the FL pulse rate at a rate near the upper limit of self-starting rate of stepping motor. Set a desired number of idling pulses with R10. If you set it at n (n = 1 to 7), the nth pulse provides the timing for acceleration. Setting at 0 results in the same effect as setting at 1.

In the case of n = 0 or 1



In the case of n = 3



- Number of idling pulses
  Write a desired number of idling pulses in bits 10 to 8 of R10. The setting range is 0 to 7. The PCL5022 will start acceleration after outputting pulses to that number at the FL pulse rate.
- You can read the idling pulse control counter through bits 22 to 20 of R13.

5.4.4 Servomotor Interface

The PCL5022 provides the following three signals for servomotor control.

(1) $\overline{\text{INP}}$

Usually, a pulse train input servomotor driver has a deviation counter to detect a deviation between input command pulses and feedback pulses and controls the motor so that the deviation is 0. Theoretically, the servomotor operates with some delay from command pulses. Accordingly, if the pulse generator stops outputting pulses, the servomotor does not stop running until the deviation counter recovers the zero status. When the counter recovers the zero status, the servo driver outputs the in-position signal to the pulse generator to indicate the motor stops running. The $\overline{\text{INP}}$ pin inputs this in-position signal.

Usually, the PCL5022 stops generating pulses upon completion of outputting pulses as designated. But by setting the RMD register, you can delay the completion of operation to the time when the $\overline{\text{INP}}$ signal is turned on. Status, $\overline{\text{BSY}}$ and $\overline{\text{INT}}$ signals are also delayed.
However, the $\overline{\text{EL}}$ or $\overline{\text{ALM}}$ signal or the completion of origin return does not cause the $\overline{\text{INP}}$ signal to delay the timing of completion. The $\overline{\text{INP}}$ signal may be a pulse signal, of which the shortest width is 48 cycles at the reference clock (5μs with a clock frequency of 9.8304MHz). By turning the external input filter off, you can make the pulsewidth two cycles at the reference clock (0.2μs with a reference clock of 9.8304MHz).

- To let the PCL5022 delay the completion of pulse output until receiving $\overline{\text{INP}}$ signal
  Set bit 7 of the RMD register at 1.
  The PCL5022 will delay the completion of pulse output until the $\overline{\text{INP}}$ signal is on. Status $\overline{\text{BSY}}$ and $\overline{\text{INT}}$signals are also delayed but the $\overline{\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or origin return will stop the PCL5022 immediately without any delay.

- To select the $\overline{\text{INP}}$ signal input logic
  Set bit 3 of R9 at—
  0: negative logic
  1: positive logic

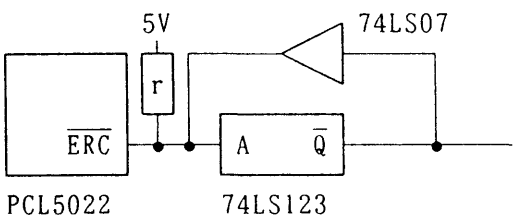
- To check ON/OFF status of $\overline{\text{INP}}$ signal, read bit 5 of R15.
  0: $\overline{\text{INP}}$ signal OFF
  1: $\overline{\text{INP}}$ signal ON

- External input signal filter
  Set bit 8 of R9 at—
  0: Minimum pulsewidth is 48 cycles at the reference clock
  1: OFF

(2) $\overline{\text{ERC}}$

Since the servomotor operates with some delay from pulses generated from the PCL5022, it keeps operating by responding to pulses remaining in the deviation counter of the driver if the $\overline{\text{EL}}$ signal or the completion of origin return stops the PCL5022 from outputting pulses. The $\overline{\text{ERC}}$ signal allows you to immediately stop the servomotor by resetting the deviation counter to zero. The $\overline{\text{ERC}}$ signal is output as a one-shot signal. The pulsewidth is a time length of 4096 cycles at the reference clock (approximately 400μs with a reference clock of 9.8304MHz). Writing the emergency stop command lets the PCL5022 output the $\overline{\text{ERC}}$ signal. By selecting automatic output of $\overline{\text{ERC}}$ signal, you can let the completion of $\overline{\text{EL}}$ signal, or $\overline{\text{ALM}}$ signal output the ERC signal to immediately stop the servomotor.

Some servo drivers require the $\overline{\text{ERC}}$ signal to have a time width of 400μs or longer. If you make such connection that the extended signal by a one-shot IC or the like is fed back to the $\overline{\text{ERC}}$ pin through an open collector output (TTL 7407 or the like), the timing of starting the timer to let the $\overline{\text{ERC}}$ recover the OFF status is delayed and the status monitor (R15) provides the pulsewidth extended signal.

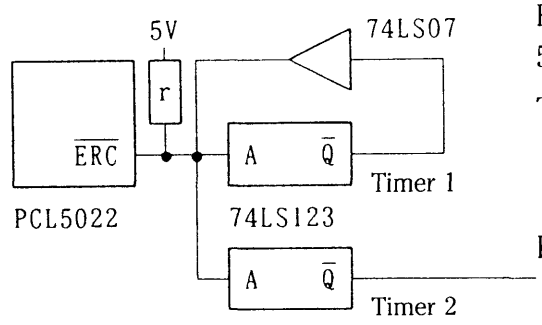


Resistance in a range of 5kΩ to 10kΩ

Extended $\overline{\text{ERC}}$ signal

Take care that the servo driver may not immediately accept command pulses if the $\overline{\text{ERC}}$ signal recovers the OFF status. By setting the $\overline{\text{ERC}}$ signal OFF timer, you can delay the start by 4096 cycles at the reference clock from writing the start command after the $\overline{\text{ERC}}$ signal recovers the OFF status.

If a time length of over 400μs is required for the $\overline{\text{ERC}}$ signal to recover the OFF status, connect two timers as shown below.



Resistance in a range of 5kΩ to 10kΩ

Timer 1 setting = Timer 2 setting + Recovery time

Extended $\overline{\text{ERC}}$ signal

- Automatic output of $\overline{\text{ERC}}$ signal
  Set bit 9 of R9 at 1. The $\overline{\text{ERC}}$ signal will be automatically output when $\overline{\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or origin return stops the PCL5022 from outputting pulses.
- $\overline{\text{ERC}}$ signal OFF timer
  Set bit 11 of R10 at 1. The PCL5022 will start with a delay of 4096 cycles at the reference clock after the $\overline{\text{ERC}}$ signal is off.
- To check ON/OFF status of $\overline{\text{ERC}}$ pin, read bit 4 of R15.
  0: $\overline{\text{ERC}}$ pin OFF
  1: $\overline{\text{ERC}}$ pin ON

(3) $\overline{\text{ALM}}$

The $\overline{\text{ALM}}$ pin receives the alarm signal output from the servo driver. The signal immediately stops the PCL5022 from generating pulses or stops it after deceleration. You can change the input logic by setting R9. Whether or not the PCL5022 is generating pulses, the $\overline{\text{ALM}}$ signal lets it output the $\overline{\text{INT}}$ signal.

If the $\overline{\text{ALM}}$ signal is in the ON status at the start, the PCL5022 outputs the $\overline{\text{INT}}$ signal without generating any command pulse. The $\overline{\text{ALM}}$ signal may be a pulse signal, of which the shortest width is a time length of 48 cycles at the reference clock (5μs with a reference clock of 9.8304MHz). By turning the external input filter off, you can make the pulsewidth 2 cycles at the reference clock (0.2μs with a reference clock of 9.8304MHz).

- To select whether the $\overline{\text{ALM}}$ signal causes immediate stop or stop after deceleration, set bit 15 of RMD register at—
  0: Immediate stop
  1: Stop after deceleration
- ALM signal input logic
  Set bit 6 of R9 at—
  0: Negative logic
  1: Positive logic
- To let the $\overline{\text{ALM}}$ signal initiate the $\overline{\text{INT}}$ signal, set bit 2 of R11 at 1.
- To check the interrupt factor, read bit 4 of R12. If it is 1, the $\overline{\text{ALM}}$ signal is the interrupt factor.
- To check ON/OFF status of $\overline{\text{ALM}}$ signal, read bit 22 ('a' axis) or bit 30 ('b' axis) of status.
  0: OFF
  1: ON
- To select the external signal input filter mode, set bit 8 of R9 at—
  0: Minimum pulsewidth 48 cycles at the reference clock
  1: OFF

5.4.5 Manual Pulser Input

For manual operation of a device, you may use a manual pulser such as a rotary encoder. The PCL5022 can input signals from the pulser and output corresponding pulses from the $\overline{OUT}$ and DIR pins, thereby allowing you to simplify the external circuit and control the present position of axis. The manual pulser input is effective between the start of constant-speed operation at the FH pulse rate and the cessation by the immediate stop command in the continuous mode 2 and between the start of constant-speed operation at the FH pulse rate and the completion of operation in the preset mode 2. Also, the microstep control is effective for the pulser input.

The PCL5022 receives plus and minus pulses or 90° phase difference signals from the pulser at PA and PB pins. The 90° phase difference signals can be input through multiplication by 1, 2 or 4. Also, one pulser may be used for 'a' and 'b' axes while internally alloting the signals appropriately to two axes.

In the continuous mode 2, the moving direction of PCL5022 depends on the rotating direction of pulser. But in the preset mode 2, the moving direction of PCL5022 is as written in the RMD register and has no concern with the rotating direction of pulser.

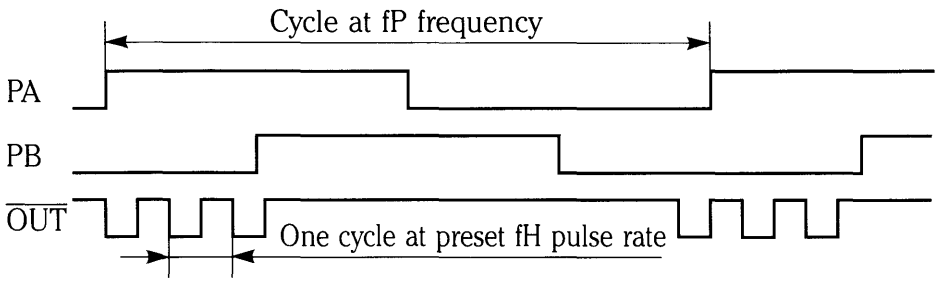
If the PCL5022 inputs 90° phase difference signals in the continuous mode 2, the moving direction is plus when the phase of the signal to the PA pin advances over that to the PB pin. In the case of two-pulse input, the PCL5022 moves in the plus direction at the edge of PA input changing from low to high.

The PCL5022 outputs the $\overline{INT}$ signal if levels of PA and PB signals change simultaneously. A maximum input frequency of pulser signals is limited by the FH pulse rate. Relations between the FH pulse rate "fH" (pps) and the pulser input frequency "fP" (pps) should be as follows.

n = Unit number of output pulses set by R10

PA & PB Input Mode	Applicable Range
1 time multiplied 90° phase difference signal	fP < fH/(n +1)
2 times multiplied 90° phase difference signal	fP < fH/[(n +1) x 2)]
4 times multiplied 90° phase difference signal	fP < fH/[(n +1) x 4)]
2-pulse input	fP < fH/(n +1)

Example: If 1 time multiplied 90° phase difference signals are input with the unit number of output pulses set at 3 (set number = 2)



- To check the interrupt factor, read bits 14 of R9. If it is 1, the interrupt factor is a simultaneous change of PA and PB inputs or the input frequency exceeding the maximum.
- To select the PA/PB input mode, set bits 13 and 12 of R9 at—
  00: 1x 90° phase difference signals
  01: 2x 90° phase difference signals
  10: 4x 90° phase difference signals
  11: Up/down two pulses
- To select the pulser input mode for 'a' and 'b' axes, set bit 31 of R9 at—
  0: Independent input to 'a' and 'b' axes
  1: Common input to 'a' and 'b' axes. The PA/PB input mode is as set for the 'a' axis.
  Pulse signal is input to the PA and PB pins of 'a' axis and the input setting is made with the pins of 'b' axis.
  Settings: 'a' axis pulser control
  Valid with PAb = high
  Invalid with PAb = low
  'b' axis pulser control
  Valid with PBb = high
  Invalid with PBb = low

5.4.6 Up/Down Counter

The PCL5022 has a 28-bit binary up/down counter for managing the present position. The counter counts output pulses or signals input to EA and EB pins. When counting signals input to EA and EB pins, it counts plus and minus pulses or 90° phase difference signals. 90° phase difference signals may be those multiplied by 1, 2 or 4. When counting output pulses, it counts them at each full-step position even under microstep control. To let it count EA and EB signals under microstep control, input these signals with a resolution of the full-step position. You can set so that a simultaneous change of EA and EB signals lets the PCL5022 output the $\overline{\text{INT}}$ signal.

If the up/down counter is set to OFF or if the PCL5022 is placed in the timer mode with output pulses selected for the counter input, the up/down counter does not operate.

The following operations reset the up/down counter to zero.
(1) Writing the counter clear command
(2) The $\overline{\text{CLR}}$ pin for up/down counter clear changes from high to low level (may cause $\overline{\text{INT}}$ signal output).
(3) Completion of origin return if so set
(4) Writing 0 in R8

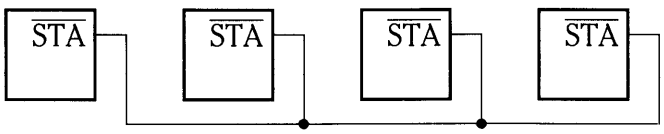
- To select whether or not to operate the up/down counter, set bit 9 of the RMD register at—
  0: Operates
  1: Does not operate
- To select the type of input signal to the up/down counter, set bit 20 of R9 at—
  0: Output pulses
  1: EA and EB input signals; EA/EB input error initiates the $\overline{INT}$ signal.
- To check the interrupt factor, read bit 12 of R12. If it is 1, it indicates that EA and EB inputs changed simultaneously.
- To select the EA/EB input mode, set bits 11 and 10 of R9 at—
  00: 1x 90° phase difference signals
  01: 2x 90° phase difference signals
  10: 4x 90° phase difference signals
  11: Plus and minus pulses
- To let the completion of origin return reset the up/down counter, set bit 6 of R10 at 1.
- To let the $\overline{CLR}$ signal initiate the $\overline{INT}$ signal, set bit 19 of R11 at 1.
- To check the interupt factor, read bit 19 of R12. If it is 1, it indicates tht the $\overline{CLR}$ signal is input, thereby resetting the up/down counter.
- To check ON/OFF status of CLR pin, read bit 6 of R16.
  0: OFF
  1: ON

5.4.7 Simultaneous Start

If you use multiple units of PCL5022, you can connect their $\overline{STA}$ pins together to start multiple motors simultaneously. In addition, you can let the PCL5022 output the $\overline{INT}$ signal at the simultaneous start.
You can also start multiple units simultaneously by driving the $\overline{STA}$ signal line with an output of open collector (74LS06 or the like).

Also, under the condition where $\overline{STA}$ pins are connected each other, you can start each axis individually. The input mode of $\overline{STA}$ pin can be selected from level trigger and edge trigger.

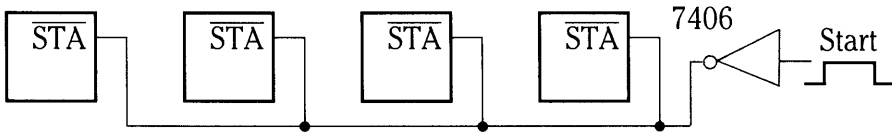
(1) Connection for Simultaneous Start with Internal Signal



- Write operation parameters and the start retention command in each unit of PCL5022. Then write the simultaneous start command in any of the units. The units in which the start retention command has been written will start generating pulses simultaneously.

- If you write an ordinary start command after writing operation parameters, only the concerned PCL5022 starts generating pulses.
- The simultaneous start command is effective for all $\overline{STA}$ pins connected.

(2) Connection for Simultaneous Start through External Circuit



The $\overline{STA}$ signal is output from the open collector. Use a one-shot signal, of which the pulsewidth should be 8 cycles or over at the reference clock.

Write operation parameters and the start retention command in each unit of PCL5022. Then an input of external start signal will start all units in which the start retention command has been written. The internal simultaneous start command too is effective under this connection.

NOTE: If you write the start retention command with the $\overline{STA}$ pin at low level, all units of PCL5022 start generating pulses immediately. To cancel the start retention status, write the immediate stop command (retention cancel).

- To select the $\overline{STA}$ signal trigger mode, set bit 23 of R9 at—
  0: Level trigger
  1: Edge trigger
- To let the $\overline{STA}$ accompany the $\overline{INT}$ signal, set bit 15 of R11 at 1.
- To check the interrupt factor, read bit 15 of R12. If it is 1, it indicates that the PCL5022 was started with the $\overline{STA}$ signal.
- To check ON/OFF status of $\overline{STA}$ pin, read bit 10 of R15.
  0: OFF
  1: ON
- To check the start retention status, read operation status bits 5 to 3 and 2 to 0.
  Bits 2 to 0=001: 'a' axis in start retention status
  Bits 5 to 3=001: 'b' axis in start retention status
- Simultaneous start command
  Writing the simultaneous start command lets the $\overline{STA}$ pin output one-shot pulse with a width of 512 cycles at the reference clock. Operation is the same in no concern with designation of the axis.
  Bit control command (HEX)

'a' axis	'b' axis	a/b
30	B0	70

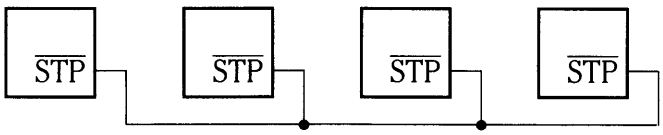
5.4.8 Simultaneous Stop

If you use multiple units of PCL5022, connect $\overline{STP}$ pins of all units. Then you can stop all units simultaneously upon abnormal stop of any unit. Also, you can let the $\overline{STP}$ signal initiate the $\overline{INT}$ signal output. Causes of abnormal include $\overline{\pm EL}$ signal, $\overline{ALM}$ signal, out-of-step detection and $\overline{SD}$ signal.

The RMD register allows you to select the simultaneous stop signal input function, the simultaneous stop signal output function and the stop method. By setting these functions, you can place the system in a condition similar to the condition where $\overline{STP}$ pins are not connected or let the PLC5022 output the $\overline{STP}$ signal at an abnormal event or stop after deceleration. signal at an abnormal stop.

In addition, you can stop all units simultaneously with an external hardware signal by driving the $\overline{STP}$ signal line through an output of open collector (74LS06 or the like).

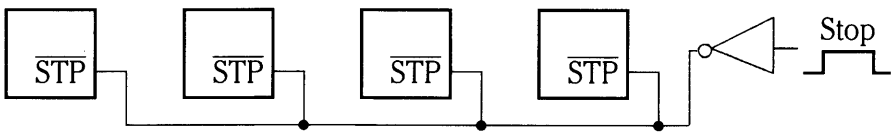
(1) Connection for Simultaneous Stop with Internal Software Signal



Set bits 13 of the RMD register at 1, set the $\overline{STP}$ input function to ON and the $\overline{STP}$ output function to ON by setting bit 14 t 1 with all units of PCL5022 to effect the simultaneous stop.

When any unit stops due to an abnormal event, all other units which are set to ON stop generating pulses.

(2) Connection for Simultaneous Stop through External Circuit



The $\overline{STP}$ signal is controlled by the open collector output. Use a one-shot signal, of which the pulsewidth should be eight cycles or over at the reference clock. The PCL5022 stops generating pulses when the $\overline{STP}$ pin changes from high to low level.

Set bit 13 of the RMD register at 1 to effect the simultaneous stop function of the concerned units of PCL5022.
Under this configuration, either external stop signal or internal stop signal stops all concerned units of PCL5022.

NOTE: If the $\overline{STP}$ pin is at low level, writing the start command does not start the PCL5022 of which the simultaneous stop function is turned on.
The $\overline{STP}$ signal for an abnormal stop due to $\overline{SD}$ or $\overline{ALM}$ signal for deceleration-stop is output after deceleration-stop.

- To select the simultaneous stop signal input function, set bit 13 of the RMD register at—
  0: OFF (invalid)
  1: ON (valid)
- To select the simultaneous stop signal output function for abnormal stop, set bit 14 of the RMD register—
  0: No $\overline{STP}$ signal output at anormal stop
  1: $\overline{STP}$ signal output at abnormal stop
- To select whether the $\overline{STP}$ signal immediately stops the PCL5022 or stops it after deceleration, set bit 15 of the RMD register at—
  0: Immediate stop
  1: Deceleration-stop
  (Common to the setting for ALM signal)
- To output the $\overline{INT}$ signal when the $\overline{STP}$ signal stops the PCL5022. set bit 3 of R11 at 1.
- To check the interrupt factor, read bit 5 of R12. If it is 1, it indicates that the $\overline{STP}$ signal stops the PCL5022.
- To check the $\overline{STP}$ pin status, read bit 11 of R15.
  0: $\overline{STP}$ pin OFF
  1; $\overline{STP}$ pin ON
- Simultaneous stop command
  Writing the simultaneous stop command lets the STP pin output one-shot pulse of which the pulsewidth is 512 cycles at the reference clock. Operation is the same in no concern with designation of the axis.
  Bit control command (HEX)

'a' axis	'b' axis	a/b
38	B80	78

5.4.9 Dummy Operation

You can let the PCL5022 perform all activities except for pulse generation. This allows you to check the PCL5022 without moving the machine.

In the dummy operation, $\overline{OUT}$ and DIR pins do not output any pulse except in the common pulse mode where the PCL5022 outputs a direction signal if it is available at the DIR pin. $\overline{\pm EL}$, $\overline{\pm SD}$ and $\overline{ALM}$ have no function.

The up/down counter inputs "output pulses" irrespective of setting of the R9 register.

In the origin return mode, the PCL5022 completes the dummy operation without outputting any pulse.

The $\overline{INT}$ signal does not delay the timing of the completion of operation.

- To effect the dummy operation, set bit 7 of R10 at 1.

5.4.10 External Input Signals from Mechanical System

The PCL5022 can input the following five signals as position detecting signals from the mechanical system.

(1) $\overline{+EL}$ and $\overline{-EL}$ Signals

The EL signal in the moving direction (+EL signal in moving in plus direction) immediately stops PCL5022 from generating pulses (may output the $\overline{INT}$ signal) and thereafter keeps it stopped if the signal recovers the OFF status. If you write the start command with this signal ON, the PCL5022 does not start generating pulses for that direction while outputting $\overline{the}$ INT signal.

$\overline{+EL}$ and $\overline{-EL}$ signals may be pulse signals, of which the shortest width is usually a time length of 48 cycles at the reference clock (approximately 5μs with a reference clock of 9.8304MHz). However, you can make it a time length of 2 cycles at the reference clock (approximately 0.2μs with a reference clock of 9.8304MHz) by turning the input filter off. The microstep control, if used, delays the stop timing until all pulses in the unit number are output. However you can stop PCL5022 before outputting all pulses in the unit number by setting bit 12 of R10 at 1.

You can check ON/OFF status of these signals by reading the status code. Also, note that these signals are neglected in the timer mode and dummy operation but the status can be monitored. You can change the input logic with the ELL pin.

- To select the input logic, set the ELL pin at—
  High level: Positive logic, Low level: Negative logic
  The ELL pin is provided for each of 'a' and 'b' axes. ELLa pin (pin 30) is for the 'a' axis and ELLb pin (pin 31), for the 'b' axis.
- To let ±EL signal output the INT, set bit 0 of R11 at 1.
- To check the interrupt factor, read bits 1 and 0 of R12.
  Bit 0=1: $\overline{+EL}$ signal stops the PCL5022.
  Bit 1=0: $\overline{-EL}$ signal stops the PCL5022.
- To check $\overline{\pm EL}$ signal status, read status bits 17 and 16 ('a' axis) or bits 24 and 23 ('b' axis).
  Bit 16 or 24=1: $\overline{+EL}$ signal ON
  Bit 17 or 25=1: −EL signal ON
- To select the external signal input filter mode, set bit 8 of R9 at—
  0: Minimum pulsewidth 48 cycles at the reference clock
  1: External signal input filter OFF

(2) $\overline{+SD}$ and $\overline{-SD}$ Signals

When the $\overline{SD}$ signal in the moving direction is turned on during varied-speed operation, the PCL5022 decelerates the pulse output to the FL rate. If the signal is turned off during or after deceleration, the PCL5022 accelerates the pulse output. By setting the RMD register, you can make the function valid or invalid.

If the signal is on at the start, the PCL5022 started for varied-speed operation does not accelerates the pulse output and continues outputting pulses at the FL rate. Also, the $\overline{SD}$ signal has no function in the constant-speed operation at the FH pulse rate.

The default input logic is negative. However, you can make it positive by setting the R9 register. The level input or latch input can be selected. The latched input is released by starting to the reverse direction or cancelling the latch input setting. By reading the status code or R15 register, you can monitor the signal (with latch or without latch).

You can also let the $\overline{SD}$ signal stop the PCL5022 after deceleration by setting. In such a case, the $\overline{SD}$ signal lets the PCL5022 in the varied-speed operation decelerate the pulse output to the FL rate and then stop it. If the $\overline{SD}$ signal is turned off during deceleration, the PCL5022 accelerates the pulse output but it does not restart if the signal is turned off after the PCL5022 stops generating pulses. Also, note that the $\overline{SD}$ signal immediately stops the PCL5022 in the constant-speed operation at the FL rate but the signal has no function in the constant-speed operation at the FH pulse rate.

- To make the $\overline{\pm SD}$ signal control valid or invalid, set bit 6 of the RMD register at 1.
- To select transaction to the $\overline{\pm SD}$ signal, set bit 22 of R9 at—
  0: Deceleration to the FL pulse rate
  1: Stop after deceleration
- To select the input logic of $\overline{\pm SD}$ signal, set bit 4 of R9 at—
  0: Negative
  1: Positive
- To select the input mode of $\overline{\pm SD}$ signal, set bit 24 of R9 at—
  0: Level input
  1: Latch input
  The latched condition is cancelled by starting to the reverse direction or by setting to level input.
- To let the $\overline{\pm SD}$ signal accompany the $\overline{INT}$ signal, set bit 1 of R11 at 1.
- To check the interrupt factor, read bits 3 and 2 of R12.
  Bit 2=1: $\overline{+SD}$ signal ON (signal through output in latch input too)
  Bit 3=1: $\overline{-SD}$ signal OFF

- To check ON/OFF status of $\overline{\pm SD}$ signal, read bits 19 and 18 ('a' axis) and bits 27 and 26 ('b' axis).
  Bit 18 or 26=1: $\overline{+SD}$ signal ON (latch output to latch input)
  Bit 19 or 27=1: $\overline{-SD}$ signal ON
- To select the external signal input filter mode, set bit 8 of R9 at—
  0: Minimum pulsewidth 48 cycles at the reference clock
  1: External input signal filter OFF

(3) $\overline{ORG}$ Signal

Use this signal for origin return. Motion control using this signal is available in the origin return modes 1 and 2. The default input logic is negative but you can change it to the positive logic. You can also select the level input or latch input. The latched condition is cancelled by the next start or by cancelling the latch input setting. If you need to stop the PCL5022 after counting the $\overline{EZ}$ signal, you should keep placing the $\overline{ORG}$ signal in the ON status until the PCL5022 stops. Or you should select the latch input. If you stop the PCL5022 with the $\overline{ORG}$ signal, it may be a pulse signal, of which the shortest width is usually a time length of 48 cycles at the reference clock (approximately 5μs with a reference clock of 9.8304MHz). However, you can make the pulsewidth a time length of two cycles at the reference clock (approximately 0.2μ with a reference clock of 9.8304MHz) by turning the external input filter off. You can check the signal (with latch or without latch) by reading the status code or the R15 register.

- To select the mode for which the $\overline{ORG}$ signal is effective, set bits 3 to 0 of the RMD register at—
  0010: Origin return mode 1
  0011: Origin return mode 2
- To select the input logic of $\overline{ORG}$ signal, set bit 5 of R9 at—
  0: Negative logic
  1: Positive logic
- To select the input mode of $\overline{ORG}$ signal), set bit 25 of R9 at—
  0: Level input
  1: Latch input

  Latched condition is cancelled by the next start or by setting to the level input.
- To output the $\overline{INT}$ signal upon completion of origin return, set bit 5 of R11 at 1.

- To generate the $\overline{INT}$ signal upon completion of operation with both 'a' and 'b' axes, set bit 7 of R11 for the 'a' axis at 1. When the origin return is complete with both axes, the INT signal will be output from the 'a' axis. Place both axes in the same operation mode and set bits 5 and 7 on the 'a' axis only. If the PCL5024 stops due to other factor, bits 11 and 7 of R11 for the 'a' axis is cancelled. Beside completion of origin return, it is usable for completion of preset operation.
- To check the interrupt factor, read bit 9 of R12. If it is 1, it indicates that the PCL5022 stops due to completion of origin return.
- To check ON/OFF status of $\overline{ORG}$ signal, read status bit 2 of R15.
  0: OFF (signal through output in latch input too)
  1: ON
- To check ON/OFF status of $\overline{ORG}$ signal, read status bit 20 ('a' axis) and status bit 28 ('b' axis).
  1: OFF (latch output in latch input)
- To select the condition at the completion of origin return, set bits 5 and 4 of R10 at—
  00: Stop upon $\overline{ORG}$ signal turning ON
  01: Stop after EZ counting from $\overline{ORG}$ ON
  10: $\overline{ORG}$ signal initiates deceleration and $\overline{EZ}$ counting then stops the PCL5022 from generating pulses.
  11: Setting prohibited
- To select the $\overline{EZ}$ counts at the completion of origin return, set bits 3 to 0 of R10 at—
  (counts − 1) in a range of 0 to 15.
- To select the $\overline{EZ}$ signal input logic, set bit 7 of R9 at—
  0: Negative logic
  1: Positive logic
- To check ON/OFF status of $\overline{EZ}$ signal, read bit 21 ('a' axis) and bit 29 ('b' axis).
  0: OFF
  1: ON
- To select the external signal input filter mode, set bit 8 of R9 at—
  0: Minimum pulsewidth 48 cycles at the reference clock
  1: External signal input mode OFF

5.4.11 Pulse Output Mode

You can select the common pulse mode or the 2-pulse mode and the output mode by setting the R9 register.

If you select the 2-pulse mode, the $\overline{OUT}$ pin outputs pulses to the plus

direction and the DIR pin outputs pulses to the minus direction. If you select the common pulse mode, the $\overline{OUT}$ pin output pulses in no relation with the moving direction and the DIR pin outputs a level signal for direction judgment. In the negative output logic, the high level direction judgment signal indicates plus direction and the low level signal indicates minus direction.

In the common pulse mode the motor driver requires a time from receiving the direction signal to accepting pulses. By effecting the direction switching timer, you can secure a time length of 4096 cycles at the reference clock (approximately 400μs with a reference clock of 9.8304MHz) for the time from a change of the direction signal to the output of pulses.

- To select the pulse output mode, set bit 2 of R9 at—
  0: Common pulse mode
  1: 2-pulse mode
- To select the $\overline{OUT}$ signal output logic, set bit 0 of R9 at—
  0: Negative logic
  1: Positive logic
- To select the DIR signal output logic, set bit 1 of R9 at—
  0: Negative logic
  1: Positive logic
- To select the direction switching timer operation, set bit 31 of R10 at—
  0: No delay of operation at direction switchover
  1: Start of operation at direction switchover is delayed by 4096 cycles at the reference clock

5.4.12 Interrupt Signal Output

The PCL5022 can output the $\overline{INT}$ signal to the CPU according to 21 types of factors. The $\overline{INT}$ signal is output when one or more interrupt factors occur on either 'a' or 'b' axis. If interrupt factors occur on both 'a' and 'b' axes, the $\overline{INT}$ signal is kept at low level until all interrupt factors are cleared. To judge on which axis the interrupt factor occurs, check the operation status. Write the interrupt generating conditions in the R11 register. The interrupt factors are stored at the time of interrupt occurrence and can be read from the R12 register. The interrupt status is cancelled by writing the R12 register read command. The read command transfers the interrupt factor data of R12 register to the input/output buffer and clears the bit.

For the preset mode or origin return mode, you can let the PCL5022 output the $\overline{INT}$ signal when operation on both 'a' and 'b' axes is complete. This is useful for interpolating operation or simultaneous origin return. If the interrupt is caused by completion of operation on both axes, the interrupt request of operation status and the interrupt factor of R12 register are with

the 'a' axis. If you want to make the completion of completion on both axes the interrupt factor, place both axes in the same operation mode and set bits 7 and 5 or bits 7 and 6 of R11 register of 'a' axis according to the operation mode. Note, however that if one axis stops due to some factor after another axis stops due to completion of the preset operation or origin return, the stop factor of the latter (completion of the preset operation or origin return) is kept as stored. To clear the stop factor, cancel the setting of bits 7 and 5 or bits 7 and 6 of R11 register for the 'a' axis.

R11—bit 5 = $\overline{\text{INT}}$ signal output upon completion of origin return
R11—bit 6 = $\overline{\text{INT}}$ signal output upon completion of preset operation
R11—bit 7 = Interrupt upon completion of operation on both 'a' and 'b' axes (only setting on the 'a' axis is effective.)

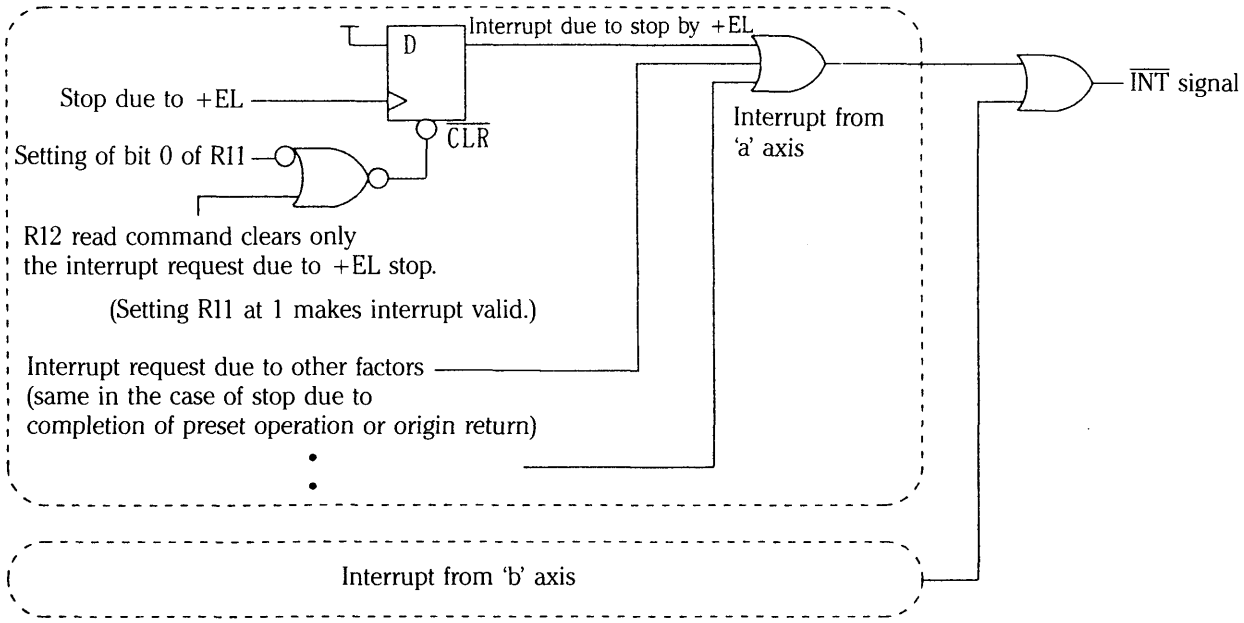
You can clear the interrupt factor by resetting the R11 register at 0 but if you do so, you cannot read the interrupt factor from the R12 register.

The $\overline{\text{INT}}$ pin requires an external pull-up register of 5kΩ to 10kΩ. Also, if you use multiple units of PCL5022, you can connect the $\overline{\text{INT}}$ pins in the wired OR mode.

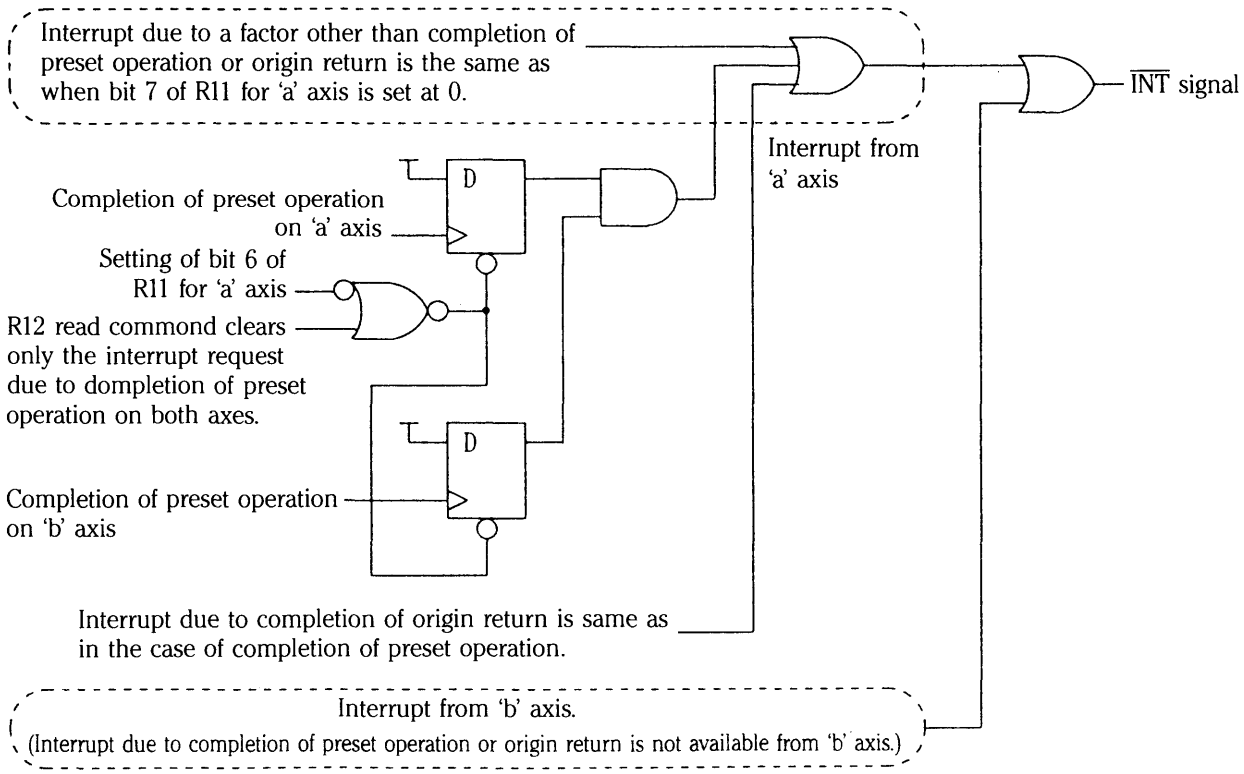
- To make completion of operation on both axes the interrupt factor, set bit 7 of R11 for the 'a' axis at 1.
  The $\overline{\text{INT}}$ signal will be output from the 'a' axis when preset operation is complete on both axes or when origin return is complete on both axes.
  To output the $\overline{\text{INT}}$ signal upon completion of preset operation on both axes, place both axes in the preset mode and sets bits 6 and 7 of R11 for the 'a' axis.
  To output the $\overline{\text{INT}}$ signal upon completion of origin return on both axes, place both axes in the origin return mode and set bits 5 and 7 of R11 for the 'a' axis.
- To check the interrupt factor on 'a' and 'b' axes, read status bit 6 ('a' axis) and bit 7 ('b' axis).
  0: One or more interrupt requests in 'a' and/or 'b' axis.
  1: No interrupt request

Equivalent Internal Circuit for Interrupt Control

(with bit 7 of R11 set at 0 for 'a' axis)



(with bit 7 of R11 set at 1 for 'a' axis)



Interrupt Signal Generating Factors

Factor	Factor (R12)	Setting (R11)	Interrupt Condition by other than R11
Stop due to $\overline{-EL}$ signal ON	Bit 0 = 1	Bit 0 = 1	
Stop due to $\overline{+EL}$ signal ON	Bit 1 = 1	Bit 0 = 1	
Deceleration-stop due to $\overline{-SD}$ signal ON	Bit 2 = 1	Bit 1 = 1	Bit 22 of R9 = 1
Deceleration-stop due to $\overline{+SD}$ signal ON	Bit 3 = 1	Bit 1 = 1	Bit 22 of R9 = 1
Stop due to $\overline{ALM}$ signal ON	Bit 4 = 1	Bit 2 = 1	
Stop due to $\overline{STP}$ signal ON	Bit 5 = 1	Bit 3 = 1	Bit 13 of RM register = 1
Stop due to out-of-step detection	Bit 6 = 1	Bits 12 to 8 $\neq$ 00000	
Stop due to command written	Bit 8 = 1	Bit 13 = 1	
Stop due to completion of origin return	Bit 9 = 1	Bit 5 = 1	Bits 5 & 7 of R11 ('a' axis) = 1 with both axes
Stop due to completion of preset operation	Bit 11 = 1	Bit 6 = 1	Bits 6 & 7 of R11 ('a' axis) = 1 with both axes
EA, EB input error	Bit 12 = 1	Bit 14 = 1	Bit 20 of R9 = 1
ERA, ERB input error	Bit 13 = 1	Bit 14 = 1 & bits 12 to 8 $\neq$ 00000	
PA, PB input error	Bit 14 = 1	Bit 14 = 1	Continuous mode 2 or preset mode 2
Start with $\overline{STA}$ signal	Bit 15 = 1	Bit 15 = 1	Start retention status
Ramping-up completed	Bit16 = 1	Bit 16 = 1	
Ramping-down started	Bit 17 = 1	Bit 17 = 1	
$\overline{CLR}$ signal input (u/d counter clear)	Bit 19 = 1	Bit 19 = 1	
AP0 pin changing from high to low	Bit 20 = 1	Bit 20 = 1	
AP1 pin changing from high to low	Bit 21 = 1	Bit 21 = 1	
AP2 pin changing from high to low	Bit 22 = 1	Bit 22 = 1	
AP3 pin changing from high to low	Bit 23 = 1	Bit 23 = 1	

5.5 Command Buffer

You can write the following commands in the command buffer.

Operation commands: To start/stop pulse output and select pulse rate
AP output control commands: To set AP pin status for output.
Bit control commands: To stop in emergencies, reset counters and set each individual bit of AP pin output
Register control command: To control communication between the CPU and registers
(CPU ↔ input/output buffer ← (register control command) → registers)

5.5.1 Operation Commands

Write the operation command to the address (No. 0 with Z80 interface) of operation command buffer. With the operation command for both axis, you can start or stop both axes or change the pulse rates simultaneously.

START COMMANDS

Write a start command when the PCL5022 stops generating pulses. Except for the simultaneous start command (7), writing a start command during pulse output in progress is invalid. Start commands include those to let the PCL5022 output remaining pulses counted by the preset counter.

(1) 10HEX for 'a' axis, 90HEX for 'b' axis, 50HEX for both axes
These commands start the PCL5022 outputting pulses constantly at the FL pulse rate.

(2) 11HEX for 'a' axis, 91HEX for 'b' axis, 51HEX for both axes
These commands start the PCL5022 outputing pulses constantly at the FH pulse rate.

(3) 13HEX for 'a' axis, 93HEX for 'b' axis, 53HEX for both axes
These commands start the PCL5022 outputting pulses at the FL pulse rate and then accelerate the pulse output to the FH pulse rate.

(4) 14HEX for 'a' axis, 94HEX for 'b' axis, 54HEX for both axes
These commands start the PCL5022 outputting pulses constantly at the FL pulse rate and if the PCL5022 is in the preset mode, let it output remaining pulses counted by the preset counter and then stop.

(6) 17HEX for 'a' axis, 97HEX for 'b' axis or 57HEX for both axes
These commands start the PCL5022 outputting pulses constantly at the FH pulse rate and if the PCL5022 is in the preset mode, let it output remaining pulses counted by the preset counter.

(7) 30HEX (B0HEX and 70HEX to the same effect)
This command lets the PCL5022 output one-shot start pulse from the $\overline{\text{STA}}$ pin to start the PCL5022 in which the start retention command is written.

START RETENTION COMMANDS

Write a start retention command when the PCL5022 stops generating pulses. The PCL5022 will be placed in a condition waiting for the $\overline{STA}$ signal. Writing a start retention command during pulse output is ineffective. You can read the retention status with the operation status code. If you write the immediate stop command under the retention status, the retention status is cancelled and the $\overline{STA}$ signal does not start the PCL5022.

(1) 20HEX for 'a' axis, A0HEX 'b' axis or 60HEX for both axes
These commands place the PCL5022 in the start retention status and the $\overline{STA}$ signal will start it outputting pulses constantly at the FL pulse rate.

(2) 21HEX for 'a' axis, A1HEX for 'b' axis, 61HEX for both axes
These commands place the PCL5022 in the start retention status and the $\overline{STA}$ signal will start it outputting pulses constantly at tho FH pulse rate.

(3) 23HEX for 'a' axis, A3HEX for 'b' axis, 63HEX for both axes
These commands place the PCL5022 in the start retention status and the $\overline{STA}$ signal will start it outputting pulses at the FL rate and then accelerate the pulse output to the FH rate.

(4) 24HEX for 'a' axis, A4HEX for 'b' axis, 64HEX for both axes
These commands place the PCL5022 in the start retention status and the $\overline{STA}$ signal will start it outputting pulses at the FL rate and if the PCL5022 is in the preset mode, let it output remaining pulses and then stop.

(5) 25HEX for 'a' axis, A5HEX for 'b' axis or 65HEX for both axes
These commands place the PCL5022 in the start retention status and the $\overline{STA}$ signal will start it outputting pulses at the FH pulse rate and if the PCL5022 is in the preset mode, let it output remaining pulses and then stop.

(6) 27HEX, A7HEX, 67HEX
These commands place the PCL5022 in the start retention status and the STA signal will start it outputting pulses at the FL pulse rate and accelerate the pulse output to the FH pulse rate. If the PCL5022 is in the preset mode, it will output remaining pulses and then stop outputting pulses.

PULSE RATE SWITCHOVER COMMANDS

Write pulse rate switchover commands when the PCL5022 is outputting pulses. Writing them during cessation is invalid.

(1) 00HEX, 80HEX, 40HEX
These commands immediately switch the pulse rate to the FL pulse rate.

(2) 01HEX, 81HEX, 41HEX
These commands immediately switch the pulse rate to the FH pulse rate.

(3) 02HEX for 'a' axis, 82HEX 'b' axis, 42HEX for both axes
These commands let the PCL5022 decelerate the pulse output to the FL pulse rate.

(4) 03HEX, 83HEX, 43HEX
These commands let the PCL5022 accelerate the pulse output to the FH pulse rate.

STOP COMMANDS

Use the stop command to stop the PCL5022 from outputting pulses. Under microstep control, the stop timing is delayed until pulses are output to the unit number.

(1) 09HEX for 'a' axis, 89HEX for 'b' axis, 49HEX for both axes
These commands immediately stop the PCL5022 from outputting pulses. The start retention command, if written, is cancelled.

(2) 0AHEX for 'a' axis, 8AHEX for 'b' axis, 4AHEX for both axes
These commands written during constant-speed operation at the FH pulse rate or during varied-speed operation let the PCL5022 decelerate the pulse output to the FL pulse rate and then stop. If written during constant-speed operation at the FL pulse rate, the PCL5022 immediately stops outputting pulses.

(3) 38HEX (B8HEX and 78HEX to the same effect)
This signal lets the PCL5022 output one-shot stop pulse from the $\overline{\text{STP}}$ pin. The command stops the axis for which the $\overline{\text{STP}}$ input function is made valid by setting bit 13 of the RMD register at 1.

5.5.2 AP Output Control Command

Write the AP output control command to the address (No. 1 with Z80 interface) of AP output control command buffer. When pins AP0 to AP3 are set for output by setting the R9 register, the AP output control command controls all 8 bits of the buffer which holds the output status. The setting of this buffer is held irrespective of input/output setting of AP pins. You can set bit by bit with the bit control command.

5.5.3 Bit Control Commands

Write bit control commands to the address (No. 2 with Z80 interface) of bit control command buffer. Bit control commands include commands to control bits of AP pins, command for emergency stop and commands to reset counters.

AP PIN BIT CONTROL COMMANDS

If the pins AP0 to AP3 are set for output with the R9 register, you can control each bit of the buffer which holds the output status.

(1) ?0HEX for 'a' axis, A0HEX 'b' axis, 60HEX for both axes
These commands put the AP0 output pin at high level.

(2) 21HEX for 'a' axis, A1HEX for 'b' axis, 61HEX for both axes
These commands put AP1 output pin at high level.

(3) 22HEX for 'a' axis, A2HEX for 'b' axis, 62HEX for both axes
These commands put the AP2 output pin at high level.

(4) 23HEX for 'a' axis, A3HEX for 'b' axis, 63HEX for both axes
These commands put the AP3 output pin at high level.

(5) 00HEX for 'a' axis, 80HEX for 'b' axis or 40HEX for both axes
These commands put the AP0 output pin at low level.

(6) 01HEX for 'a' axis, 81HEX for 'b' axis, 41HEX for both axes
These commands put the AP1 output pin at low level.

(7) 02HEX for 'a' axis, 82HEX for 'b' axis, 42HEX for both axes
These commands put the AP2 output pin at low level.

(8) 03HEX for 'a' axis, 83HEX for 'b' axis, 43HEX for both axes
These commands put the AP3 output pin at low level.

RESET CONTROL COMMANDS

You can use the following commands to reset internal counters or for emergency stop.

(1) 09HEX for 'a' axis, 89HEX for 'b' axis, 49HEX for both axes
These commands reset the up/down counter (R8 register) to zero.

(2) 0AHEX for 'a' axis, 8AHEX for 'b' axis, 4AHEX for both axes
These commands reset the out-of-step detection deviation counter to zero.

(3) 2BHEX for 'a' axis, ABHEX for 'b' axis, 6BHEX for both axes

These commands written during pulse output immediately stop the PCL5022 from outputting pulses. Different from the immediate stop command of operation commands, these commands stop the PCL5022 in no relation with the status of output pulse. If the PCL5022 is under microstep control, thereby, it stops at any position of the unit number of output pulses and therefore the width of the last output pulse may be shorter. When the command is written, the $\overline{\text{ERC}}$ signal is output as a one-shot signal.

5.5.4 Register Control Commands

Write the register control command to the address (No. 3 with the Z80 interface) of the register control command buffer. Register control commands are used for data communication between the CPU and registers. Writing the command transfers data between the register and the input/output buffer.

The register read command copies data from the register to the input/output buffer and then lets the CPU read the data from the input/output buffer. The register write command lets the CPU write data in the input/output buffer and then the data is copied from the input/output buffer to the register.

Write the following commands to address 3 in the case of Z80 interface. Do not write any command other than listed below.

Read Command		Write Command		Subject Registers/Counters
'a' axis	'b' axis	'a' axis	'b' axis	
00HEX	80HEX	40HEX	C0HEX	R0 register (moving amount)
01HEX	81HEX	41HEX	C1HEX	R1 register (FL rate)
02HEX	82HEX	42HEX	C2HEX	R2 register (FH rate)
03HEX	83HEX	43HEX	C3HEX	R3 register (acceleration rate)
04HEX	84HEX	44HEX	C4HEX	R4 register (deceleration rate)
05HEX	85HEX	45HEX	C5HEX	R5 register (multiplication factor)
06HEX	86HEX	46HEX	C6HEX	R6 register (ramping-down point)
08HEX	88HEX	48HEX	C8HEX	R8 register (up/down counter)
09HEX	89HEX	49HEX	C9HEX	R9 register (environment setting 1)
0AHEX	8AHEX	4AHEX	CAHEX	R10 register (environment setting 2)
0BHEX	8BHEX	4BHEX	CBHEX	R11 register (environment setting 3)
0CHEX	8CHEX			R12 register (interrupt factor)
0DHEX	8DHEX			R13 register (counter monitor)
0EHEX	8EHEX			R14 register (command monitor)
0FHEX	8FHEX			R15 register (pin status monitor)
3CHEX	BCHEX			Preset counter (counter value)
3DHEX	BDHEX			Ramping-down point counter (counter value)
3FHEX	BFHEX	7FHEX	FFHEX	RMD register (operation mode)

5.6 Registers

Registers store numerical data and control parameters. If the data are the same as previous, you need not write them anew. When you read a register parameter as 32-bit data, unused high-place bits are all 0 (e.g. bits 31 to 27 of R0 register, bits 31 to 13 of registers R1 to R4).

5.6.1 R0—Output Pulse Register, 28-bit

This register sets a target position in the number of output pulses. In the timer mode, origin return mode 2, preset modes 1 and 2 and linear interpolation mode, it retains the number of output pulses in a range of 0 to 268,435,455 (FFFFFFS$_{HEX}$). The number of pulses written in this register is loaded into the preset counter at the start and the preset counter counts down the number at every pulse output. In the preset mode, the PCL5022 will stop outputting pulses when the preset counter counts down to 0. If you start the PCL5022 in the preset mode with 0 written in the this register, the PCL5022 stops immediately without outputting any pulse.

By setting the RMD register, you can stop the preset counter from counting down or start it counting when the AP3 pin changes from high to low level. Under microstep control, the preset counter counts down at every output of pulses corresponding to the resolution and, therefore, the number of output pulses is (preset counter value) x (unit number of output pulses). The unit number of output pulses will be written in the R10 register. Refer to "5.4.1 Microstep Control" for details.

- To select the operation of preset counter, set bits 12 and 11 of the RMD register at—
  00: Normal counting
  01: No counting
  10: Setting prohibited
  11: Starts counting when AP3 pin changes from high to low level.
- For the unit number of output pulses for microstep control, set bits 19 to 16 of R10 register at (resolution of microstep − 1). The setting range is 0 to 15.

5.6.2 R1—FL Pulse Rate Register, 14-bit

This register sets a starting pulse rate for varied-speed operation in a range of 1 to 16,383 (3FFF$_{HEX}$) steps. An actual FL pulse rate is a product of the R1 parameter and R5 parameter. Refer to "5.1.1 Setting Acceleration/Deceleration Pattern."

5.6.3 R2—FH Pulse Rate Register, 14-bit

This register sets an operating pulse rate in a range of 1 to 16,383 (3FFF$_{HEX}$) steps. For varied-speed operation, enter a higher value in this register than in the register R1. An actual FH pulse rate is a product of R2 parameter and R5 parameter. Refer to "5.1.1 Setting Acceleration/Deceleration Pattern."

5.6.4 R3—Acceleration Rate Register, 14-bit

For varied-speed operation, enter an acceleration parameter in a range of 1 to 16,383 (3FFF$_{HEX}$). If the ramping-down point is automatically set, the acceleration parameter written in this register is used for deceleration. Refer to "5.1.1 Setting Acceleration/Deceleration Pattern."

5.6.5 R4—Deceleration Rate Register, 14-bit

If the ramping-down point is manually set for varied-speed operation, enter the deceleration parameter in this register in a range of 16,383 (3FFF$_{HEX}$). Refer to "5.1.1 Setting Acceleration/Deceleration Pattern."

5.6.6 R5—Multiplication Factor Register, 12-bit

The parameter entered in this register is used to multiply the pulse rates entered in registers R1 and R2. The setting range is 1 to 4,095 (FFF$_{HEX}$). Refer to "5.1.1 Setting Acceleration/Deceleration Pattern."

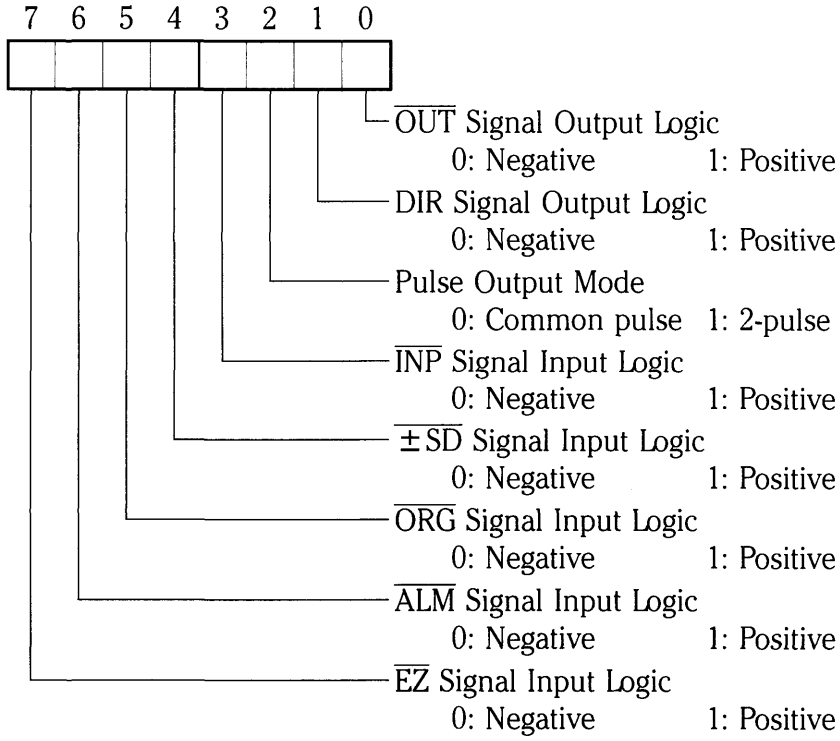
5.6.7 R6—Ramping-down Point Register, 22-bit

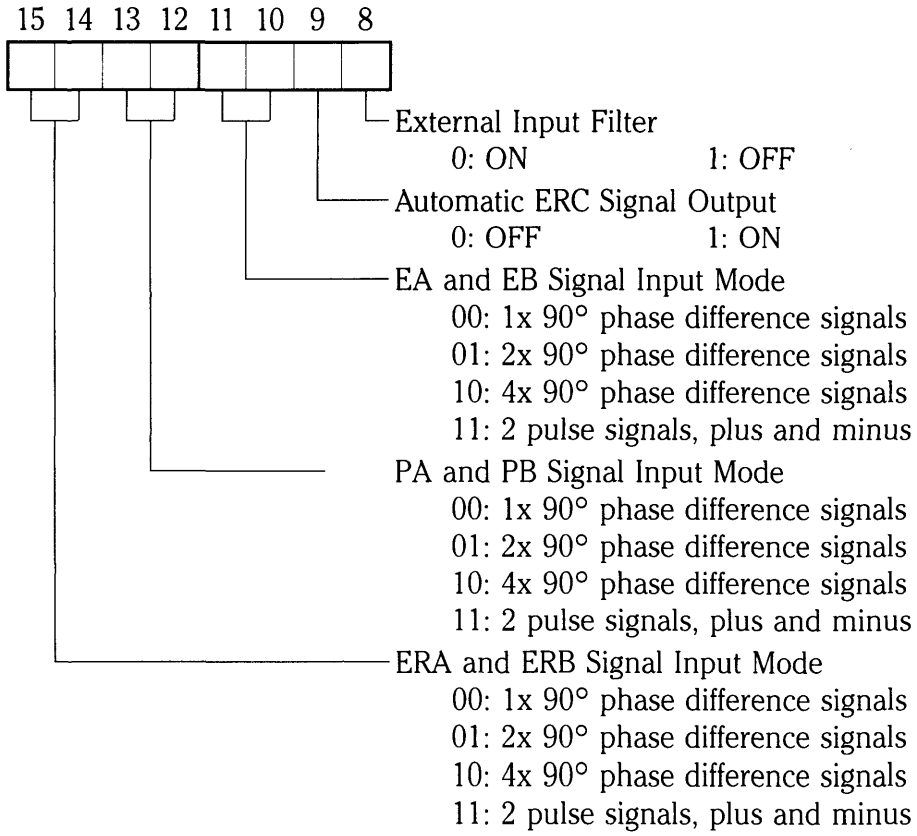
This register sets a starting point of deceleration for varied-speed operation or in-positioning in a range of 0 to 4,194,303 (3FFFFF$_{HEX}$). If the ramping-down point is manually set or if you want to shift the starting point of deceleration with the ramping-down point set automatically, write 0 in this register. Refer to "5.1.4 Setting Ramping-down Point."

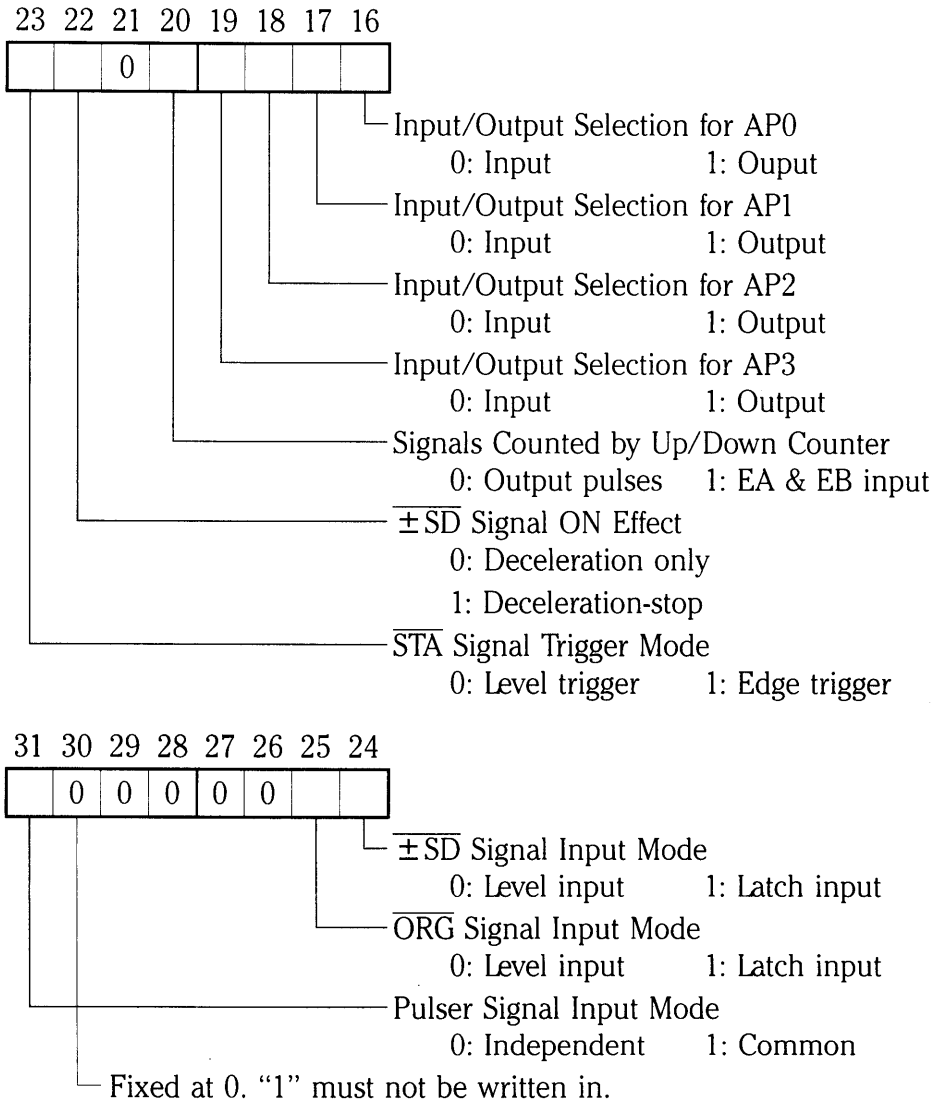
5.6.8 R8—Up/Down Counter, 28-bit

The 18-bit binary up/down counter can be used for the control of present position. The setting or counting range is 0 to 268,435,455 (FFFFFFF$_{HEX}$). Refer to "5.4.6 Up/Down Counter."

5.6.9 R9—Environmental Condition Register 1, 32-bit







Bits 7 to 0—For Setting Input/Output Logic and Pulse Output Mode

For the pulse output mode, refer to "5.4.11 Pulse Output Mode."

Bit 8—For Setting External Input Filter

To prevent erroneous operation due to noise, ±EL, ±SD, ORG, ALM and INP are input through the filter. If the bit 8 is set at 0, the PCL5022 does not accept these signals of which the pulsewidth is shorter than 48 cyles at the reference clock (approximately 5μs with a referece clock of 9.8304MHz). If the bit is set at 1, the PCL5022 accepts these signals of which the pulsewidth is longer than two cycles at the reference clock (approximately 0.2μs with a reference clock of 9.8304MHz). Set it at 1 if you need to increase the response characteristic.

Bit 9—Automatic $\overline{\text{ERC}}$ Output Function

Set bit 9 at 1. The PCL5022 will automatically output the $\overline{\text{ERC}}$ signal the $\overline{\pm\text{EL}}$ or $\overline{\text{ALM}}$ signal stops the PCL5022 or when it completes the origin return. However, if the RMD register is set to let $\overline{\text{ALM}}$ and $\overline{\text{STP}}$ signals initiate deceleration-stop, the $\overline{\text{ERC}}$ signal will be output after deceleration-stop.

Bits 11 and 10—For Setting EA and EB Signal Input Mode

Set the input mode of encoder feedback signals for present position control. In the 2-pulse input mode, counting is made at the edge of the pulse changing from low to high level.

Bits 13 and 12—For Setting PA and PB Signal Input Mode

Set the input mode of manual pulser for continuous operation. In the 2-pulse input mode, counting is made at the edge of the pulse changing from low to high level.

Bits 15 and 14—For Setting ERA and ERB Signal Input Mode

Set the input mode of encoder feedback signals for out-of-step detection. In the 2-pulse input mode, counting is made at the edge of the pulse changing from low to high level.

Bits 19 to 16—AP0 to AP3 Input/Output Mode

Define AP0 to AP3 pins as input or output, bit by bit.

Bit 20—Up/Down Counter

You can select whether the up/down counter counts either output pulses or EA and EB input signals. If you select "output pulses" for microstep control, the up/down counter will not count each output pulse but it will count in the unit number.

Bit 22—$\overline{\pm\text{SD}}$ Signal Effect

Select the operation the PCL5022 will perform when the $\overline{\text{SD}}$ signal in the moving direction is turned on. For details, refer to "5.4.10 External Input Signals from Mechanical System."

Bit 23—$\overline{\text{STA}}$ Signal Input Mode

For simultaneous start of multiple units of PCL5022, select the STA signal input mode, level trigger or edge trigger. Setting is available only for the 'a' axis.

Bit 24—$\overline{\pm\text{SD}}$ Signal Input Mode

Select the $\overline{\pm\text{SD}}$ signal input mode, level input or latch input. The latched input will be cancelled by starting in the reverse direction or switching to the level input.

Bit 25—$\overline{\text{ORG}}$ Signal Input Mode

Select the $\overline{\text{ORG}}$ signal input mode, level input or latch input. The latched input will be cancell by starting the next operation or switching to the level input.

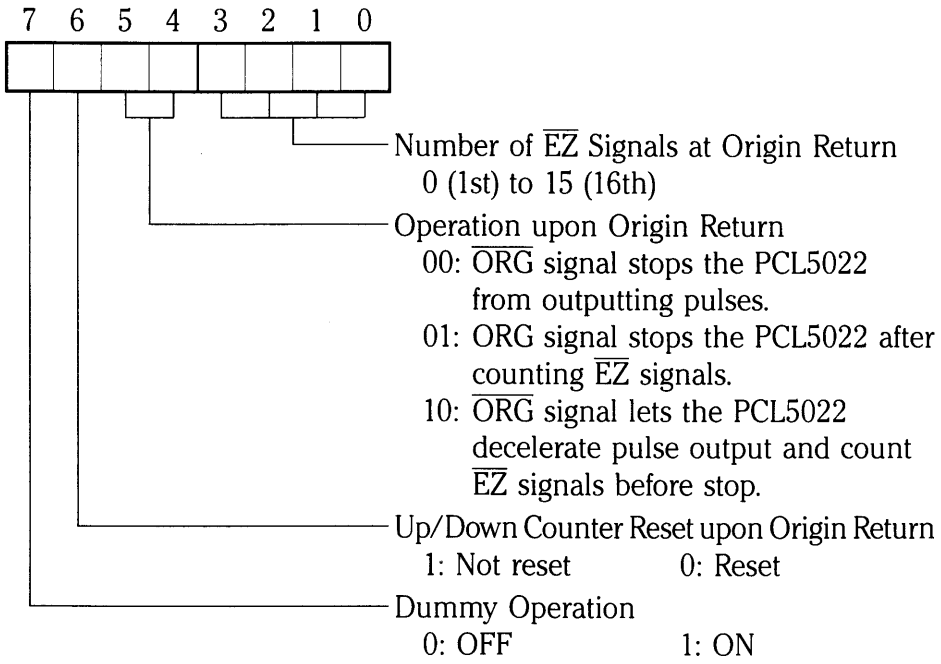
Bit 31—Pulser Signal Input

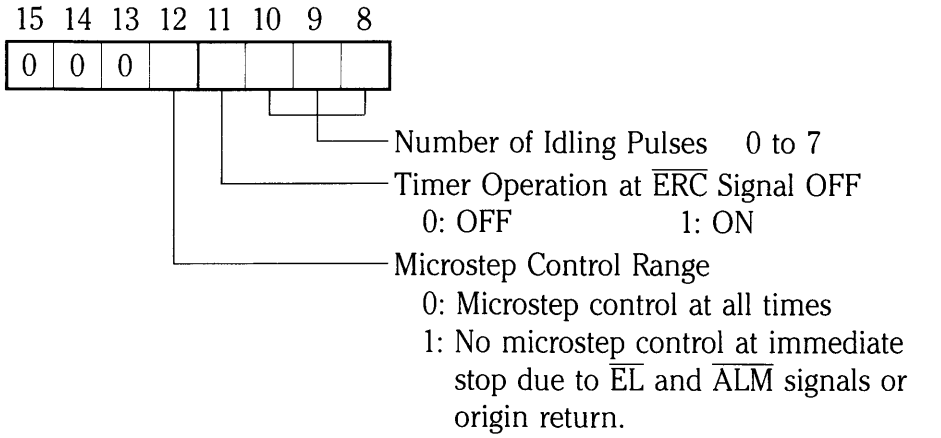
The PCL5022 can input signals from two pulsers individually for 'a' and 'b' axes or from one pulser to internally allot them to 'a' and 'b' axes. Note, however, that if you select the common input, multiplication and other settings for the 'a' axis are used; and PA and PB pins of 'b' axis are axis selection pins, that is, the PAb pin at high level makes the pulser input to the 'a' axis effective and the PBb pin at high level makes the pulse input to the 'b' axis effective.

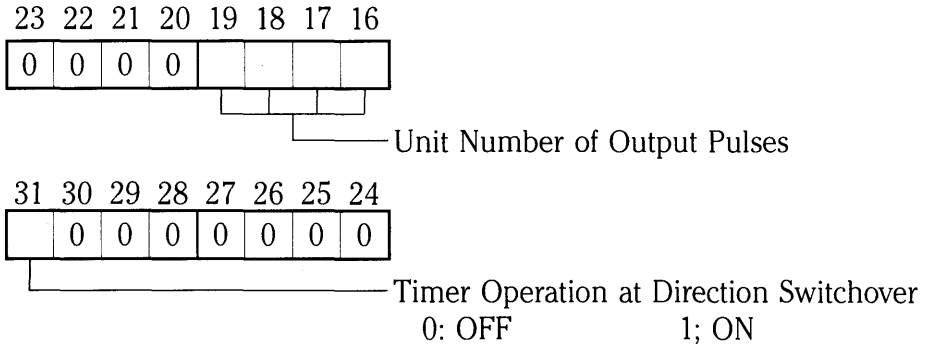
Pin Settings and Axis Selection for Common Input

PAa Pin Setting	L	H	L	L
PBb Pin Setting	L	L	H	H
Pin/s Selected	None	'a' axis	'b' axis	'a'/'b' axes

5.6.10 R10—Environmental Condition Register 2, 32-bit







Bits 3 to 0—Number of $\overline{EZ}$ Signals at Origin Return

If you set the condition of completion of origin return to "01" or "10," counting $\overline{EZ}$ signals is required to complete the origin return. Enter the 4-bit binary code in these bits. The value you enter is (number of $\overline{EL}$ signals counted − 1).

Bits 5 and 4—Operation upon Origin Return

The ORGT signal lets the PCL5022 stop outputting pulses based on the condition selected here.

Bit 6—Up/Down Counter Reset upon Origin Return

Set this bit at 1. The up/down counter will be reset to zero upon completion of origin return.

Bit 8—Dummy Operation

Set this bit at 1 to let the PCL5022 perform all operations without outputting any pulses. Refer to "5.4.9 Dummy Operation."

Bits 10 to 8—Number of Idling Pulses

Refer to "5.4.3 Idling Pulse Output."

Bit 11—Timer Operation at $\overline{ERC}$ Signal OFF

Set this bit at 1. Writing the start command will start the PCL5022 with a delay during a time length of 4.096 cycles at the reference clock from the $\overline{ERC}$ signal recovering OFF status. (Approximately 400μs with a reference clock of 9.8304MHz)

Bit 12—Microstep Control Range

Set this bit at 1. The $\overline{\pm EL}$ or $\overline{ALM}$ signal or completion of origin return will immediately stop PCL5022 from outputting pulses even at other than full-step position.

Bits 19 to 16—Unit Number of Output Pulses

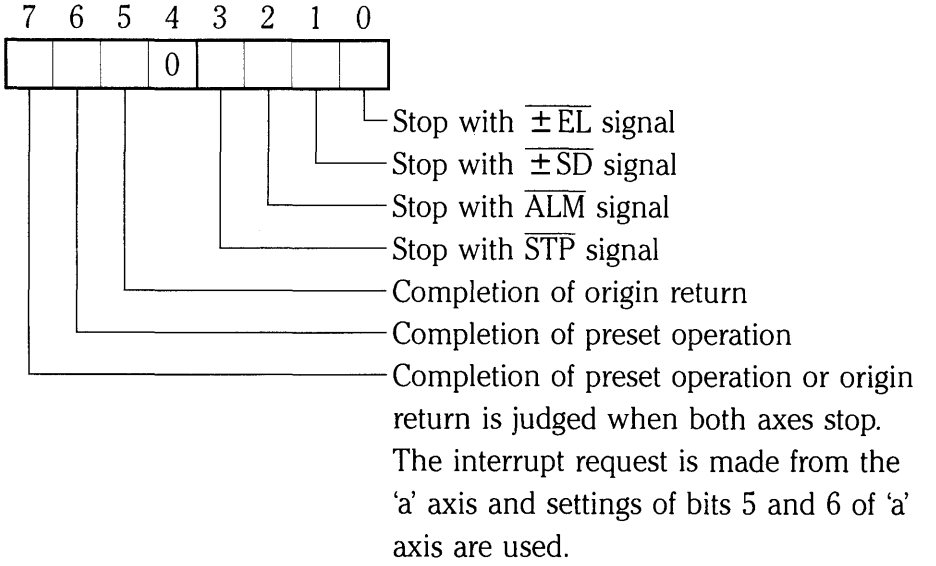
These bits set the unit number of output pulses (resolution of microstep control). The setting range is 0 to 15. If you set *n*, the unit number is (*n* + 1).

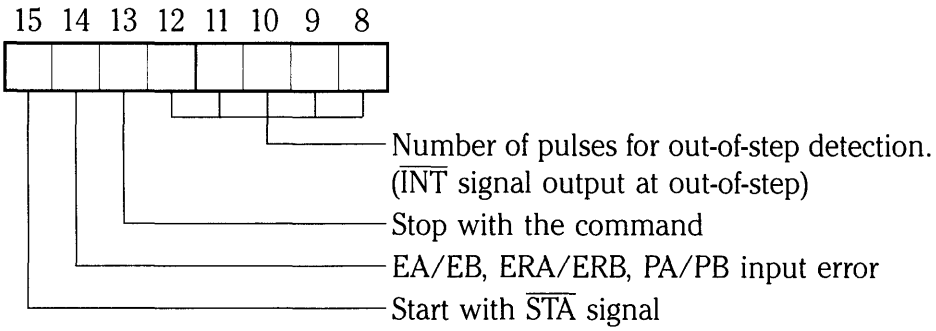
Bits 31—Timer Operation at Direction Switchover

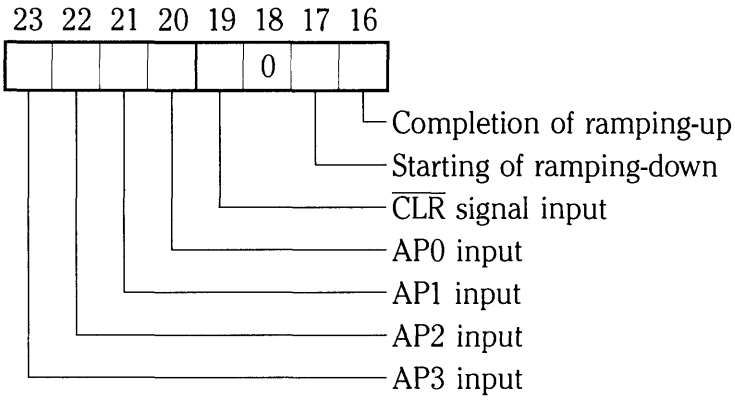
In the common pulse mode, some motor driver may require a time before accepting the pulse when the direction signal changes. Set this bit at 1. Writing the start command will delay the start of pulse output for a time length of 4,096 cycles at the reference clock from a change of direction signal.

5.6.11 R11—Environmental Condition Register 3, 24-bit

This register allows you to select factors initiating the $\overline{INT}$ signal. Enter 1 in each bit to output the signal.







Bit 0

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{\pm EL}$ signal stops the PCL5022 from outputting pulses.

Bit 1

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{\pm SD}$ signal stops the PCL5022 after deceleration with bit 22 of R9 set at 1.

Bit 2

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{\pm ALM}$ signal stops the PCL5022 from outputting pulses.

Bit 3

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{\pm STP}$ signal stops the PCL5022 after deceleration with bit 13 of RMD register set at 1.

Bit 5

Set this bit at 1. The $\overline{INT}$ signal will be output upon completion of the origin return in the origin return mode 1 or 2. If you want to output the $\overline{INT}$ signal when the origin return is complete with both 'a' and 'b' axes, set bits 5 and 7 of 'a' axis at 1. Refer to "5.4.12 Interrupt Signal Output."

Bit 6

Set this bit at 1. The $\overline{INT}$ signal will be output when the the PCL5022 completes the operation in the 1-pulse output mode, timer mode, preset mode 1 or 2 or linear interpolation mode or when it completes outputting the designated number of pulses in the origin return mode 2.

If you need to output the $\overline{INT}$ signal when the preset operation is com—plete with both 'a' and 'b' axes, set bits 6 and 7 of 'a' axis at 1. Refer to "5.4.12 Interrupt Signal Output."

Bit 7

Set this bit at 1. The preset operation or completion of origin return will be judged when the operation is complete with both axes. The interrupt request will be output from the 'a' axis.

Setting of this bit is effective only with the 'a' axis. Use this bit in combination with bits 6 and 5 of 'a' axis and in such a case, set bits 6 and 5 of 'b' axis at 0.

If you want to output the interrupt request at the time of completion of preset operation (including the linear interploation mode) on both axes, place the 'a' axis in the linear interpolation mode or place both axes in the preset mode and set bits 6 and 7 of R11 for the 'a' axis at 1.

If you want to output the interrupt request at the time of completion of origin return on both axes, place both axes in the origin return mode and set bits 5 and 7 of R11 for the 'a' axis at 1. Notice, however, that the factor which stops an axis at first will be kept as stored. Refer to "5.4.12 Interrupt Signal Output."

Bits 12 to 8—Number of Pulses for Out-of-step Detection

An out-of-step status is judged when an absolute value of the deviation counter for out-of-step detection exceeds the value written in these bits. The setting range is 0 to 31 pulses and setting at 0 makes out-of-step detection unavailable. To reset the deviation counter, write the deviation counter clear command.

Bit 13

Set this bit at 1. The $\overline{INT}$ signal will be output when the immediate stop command or deceleration-step command stops the PCL5022 from outputting pulses.

Bit 14

Set this bit at 1. The $\overline{INT}$ will be output when pins EA and EB, ERA and ERB or PA and PB change simultaneoustly, thereby resulting in an error, with these pins made valid. The $\overline{INT}$ signal will be also output when the input frequency of PA or PB signal is exceeded. Refer to "5.4.5 Manual Pulser Input."

Bit 16

Set this bit at 1. The $\overline{INT}$ signal will be output when the PCL5022 started in the varied-speed operation completes acceleration.

Bit 17

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{\pm SD}$ signal, deceleration command or coming to the ramping-down point starts the PCL5022 decelerating.

Bit 19

Set this bit at 1. The $\overline{INT}$ signal will be output when the $\overline{CLR}$ pin changes from high to low level, thereby resetting the up/down counter.

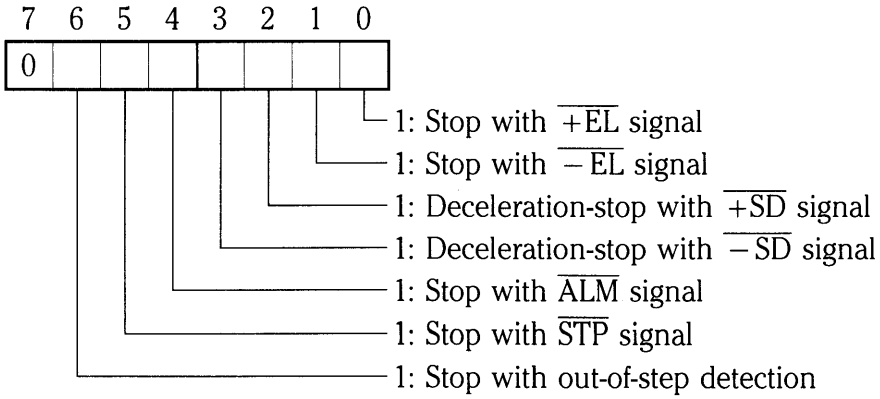
Bits 23 to 20

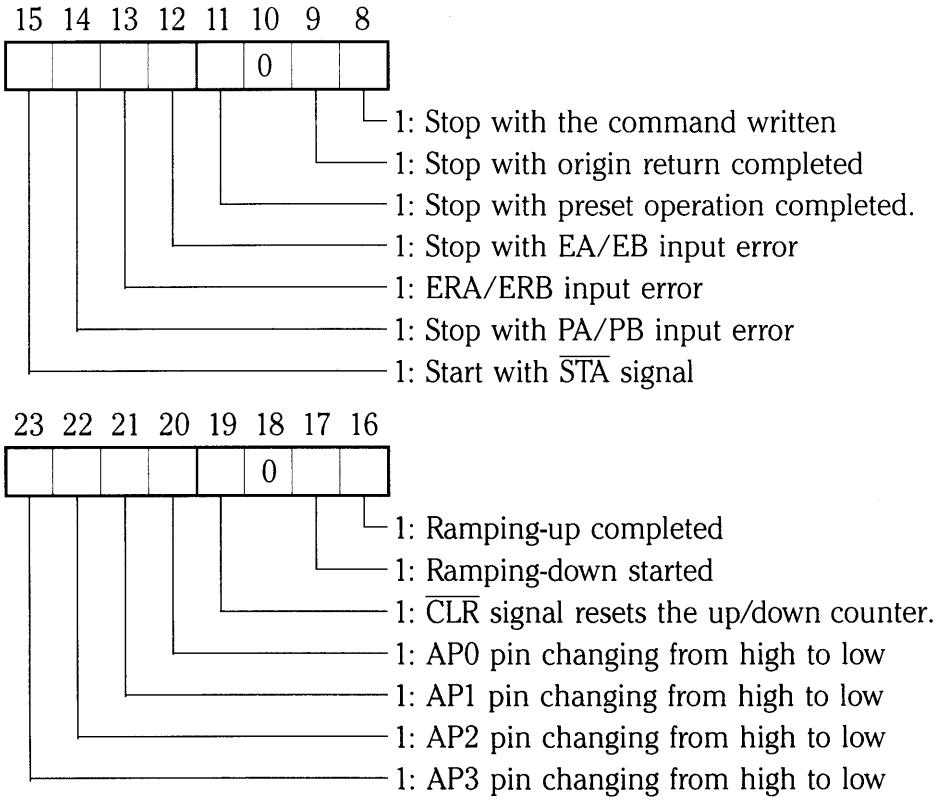
Set these bits at 1. The $\overline{INT}$ signal will be output when any pin of AP0 to AP3 changes from high to low level, whether these pins are defined as input or output.

NOTE: If you change setting of a bit from 1 to 0 when the $\overline{INT}$ signal is output due to the factor of that bit, the interrupt factor is reset. Refer to "5.4.12 Interrupt Signal Output."

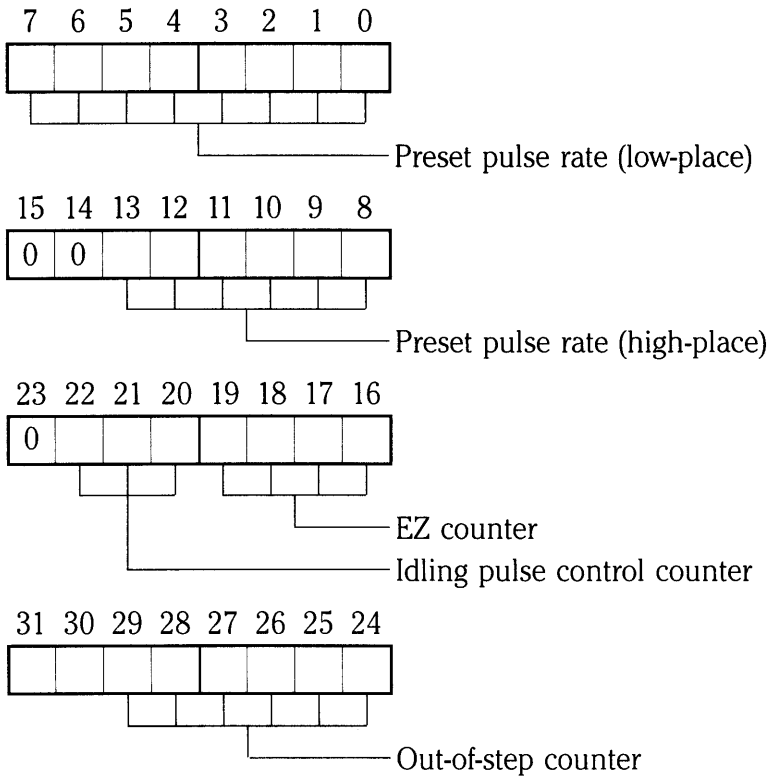
5.6.12 R12—Interrupt Factor Monitor, 24-bit

Interrupt factors are reset by reading them from this register to the input/output buffer. Check the axis which generates the interrupt factor, with the operation status code. If you restart with the limit signal ON by resetting the interrupt factor, the $\overline{INT}$ signal will be output again.





5.6.13 R13—Counter Monitor, 32-bit



Bits 15 to 0—Preset Pulse Rate

You can read the pulse rate during acceleration/deceleration in the same unit as written in R1 and R2. If you read these bits during cessation, the value is the FL pulse rate written in the R1 register.

In the linear interpolation mode, the pulse rate monitored is that of main axis. You cannot read the pulse rate of slave axis. If you read the pulse rate of 'b' axis, it is the value written in the R1 register of 'b' axis.

Bits 19 to 16—EZ Counter

Through these bits, you can read the value of EZ counter for origin return. The value is the same as the set number of EZ signals until the counting condition is satisfied. After the condition is satisfied, $\overline{EZ}$ signals let the EZ counter counts down. In the origin return for which the EZ counter is not used, the PCL5022 stops outputting pulses when the counter counts down to zero but the counter returns immediately to the initial value.

Bits 22 ti 29—Idling Pulse Control Counter

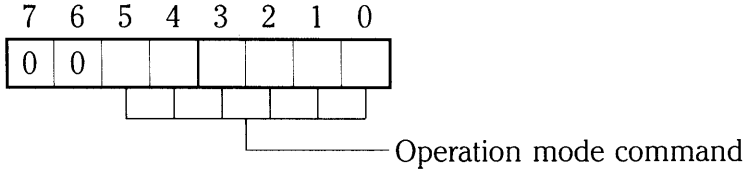
Through these bits, you can read the value of idling pulse control counter. At the cessation the value is the same as a set value. When the PCL5022 starts outputting idling pulses, it counts down every pulse output. Upon outputting the pulse which lets the counter count down to zero, the PCL5022 starts acceleration. Under microstep control, acceleration starts after outputting pulses in the number multipled by the unit number.

Bits 29 to 24—Out-of-step Counter

Through these bits, you can read the value of deviation counter for out-of-step detection. Through the counter is 6-bit with a sign, you can read the value in 8 bits extended for the sign. The value is positive when the motor is in minus direction from the position integrated by output pulses; and negative when the motor is in plus direction and it is read as a twos complement.

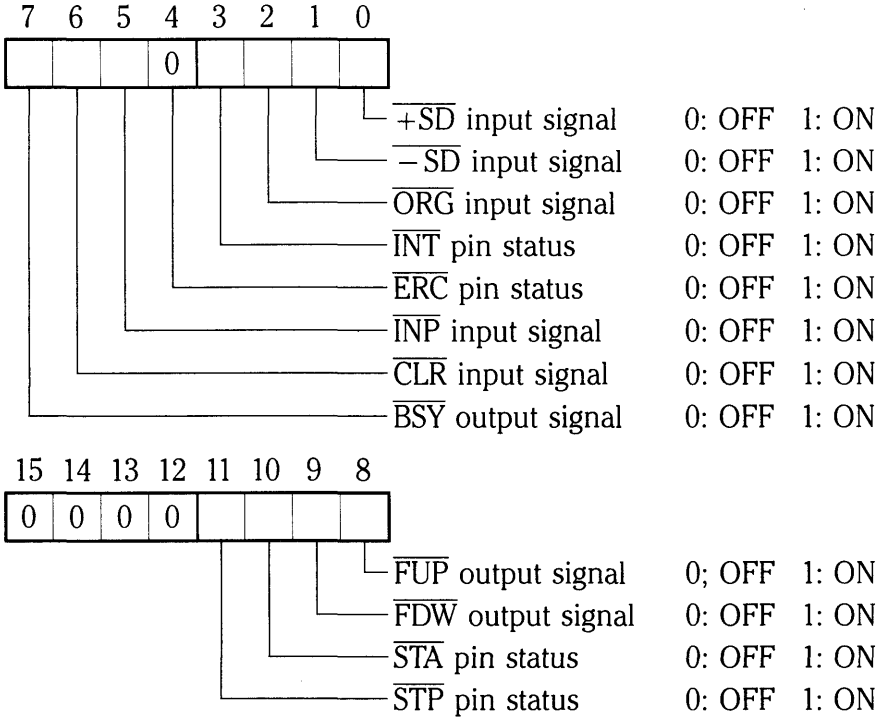
5.6.14 R14—Command Monitor, 8-bit

The R14 register allows you to read the operation command which has been written most recently, except for the simultaneous start command and simultanenous stop command.



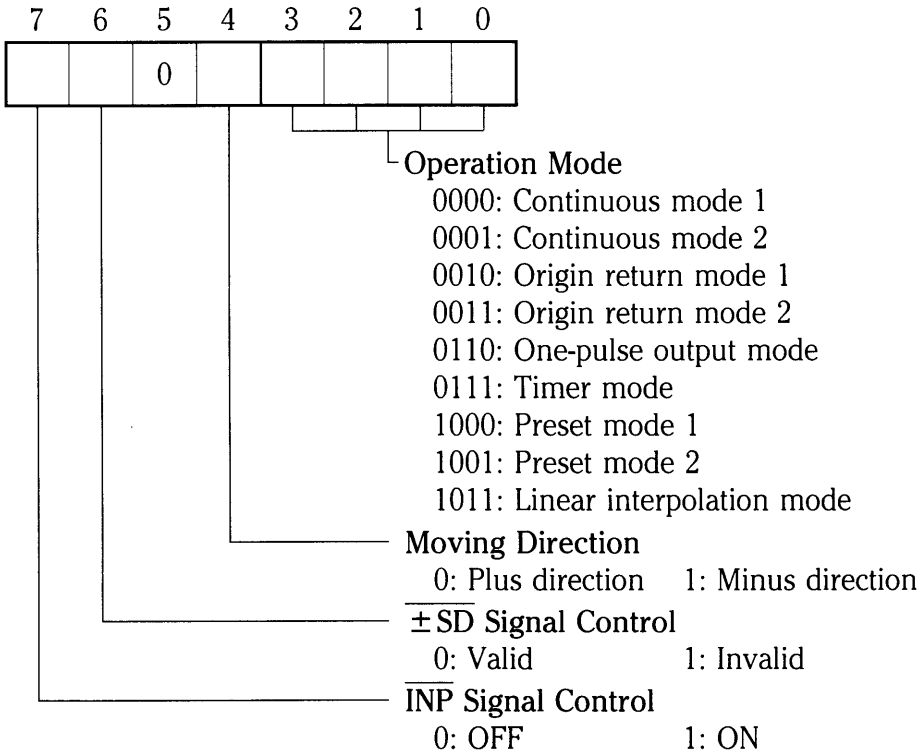
5.6.15 R15—Pin Monitor, 12-bit

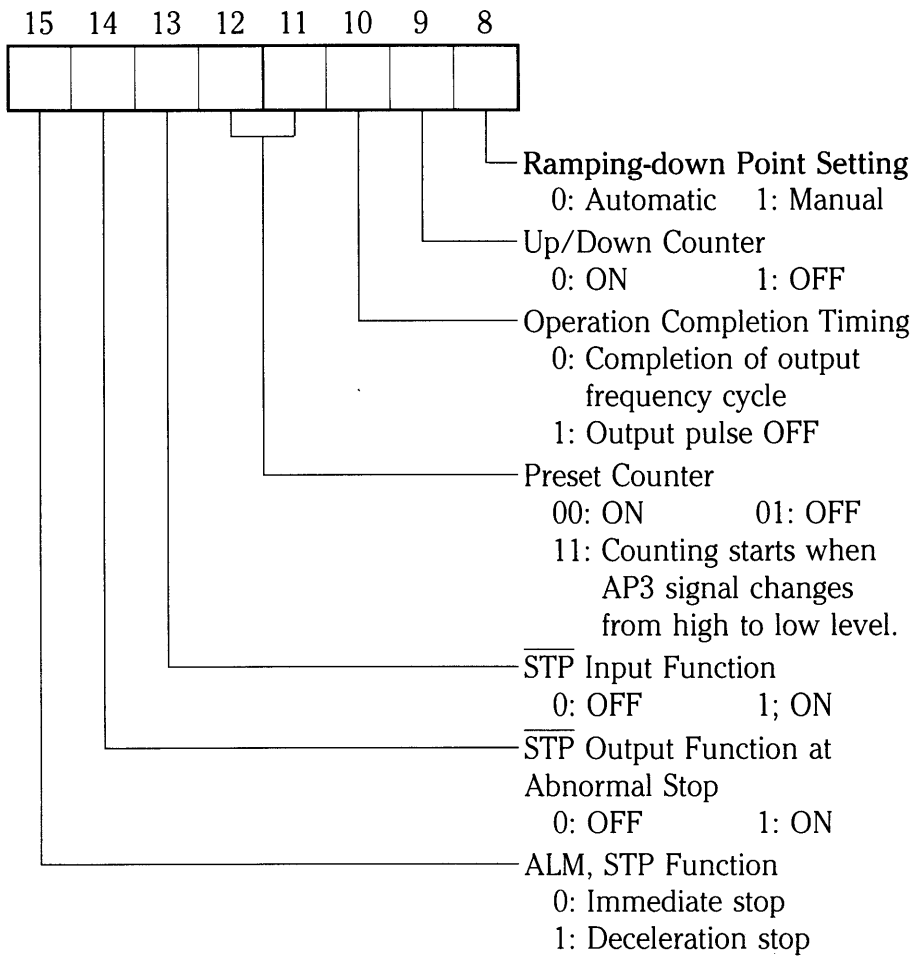
This register allows you to read the present status of each pins. With the signals for which the input/output logic can be selected by the R9 register, the ON/OFF status is read based on the set logic.



5.6.16 RMD—Operation Mode Register, 16-bit

Refer to "5.2.1 Operation Mode Register" for details.





5.7 Monitor

You can check the following by monitoring the status code.

(1) Operation Status

Operation status of 'a' and 'b' axes

Cessation of pulse output, waiting for $\overline{\text{STA}}$ signal input, delay of start, timer operation, acceleration, constant-speed operation at the FH pulse rate, deceleration, constant-speed operation at FL pulse rate, waiting for cessation of pulse output on another axis

Interrupt request from 'a' or 'b' axis

(2) ON/OFF Status of General-purpose I/O Pins for 'a' and 'b' Axis

(3) Status of 'a' Axis

$\overline{\pm\text{EL}}$,, $\overline{\pm\text{SD}}$ (with latch), $\overline{\text{ORG}}$ (with latch), $\overline{\text{EZ}}$ and $\overline{\text{ALM}}$ signal input status.

(4) Status of 'b' Axis

$\overline{\pm\text{EL}}$,, $\overline{\pm\text{SD}}$ (with latch), $\overline{\text{ORG}}$ (with latch), $\overline{\text{EZ}}$ and $\overline{\text{ALM}}$ signal input status.

(5) DParameters Retained in Registers

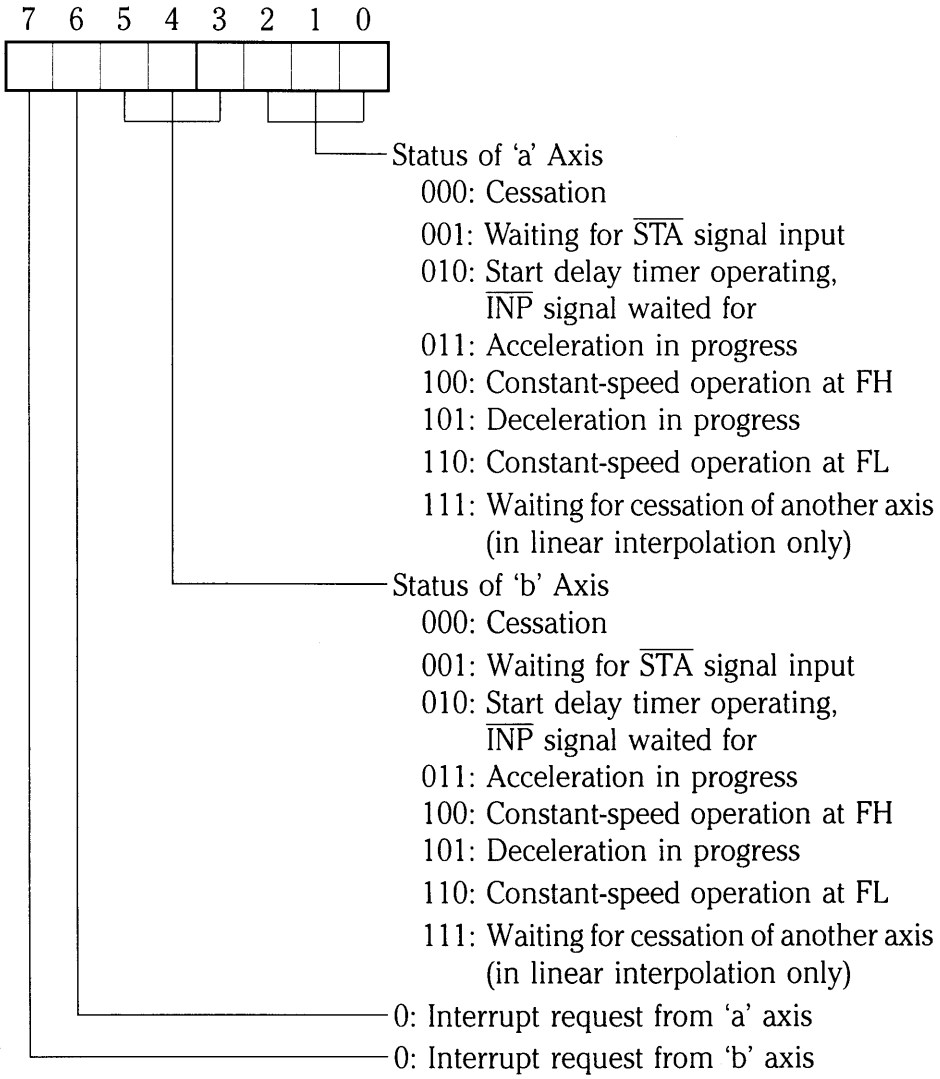
Operation mode, preset amount, FL pulse rate, FH pulse rate, acceleration rate, deceleration rate, multiplication factor, ramping-down point, up/down counter, environment settings 1, 2 and 3, interrupt factor, counter monitor, operation command monitor, pin monitor, preset counter and ramping-down point counter

5.7.1 Status

The conditions at the start of processing for status reading are latched. So contents in the data bus do not change during the read cycle. But if you read the status successively, allow a time length of over four cycles at the reference clock (approximately 0.4μs with a reference clock of 9.8304MHz).

(1) Operation Status

You can read the operation status from the address (No. 0 with Z80 interface).



Operation status of 'a' and 'b' axes

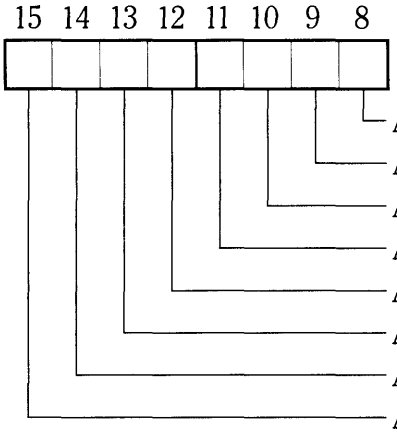
You can check the present operation status. "010" indicates: (1) $\overline{\text{ERC}}$ signal is being output, (2) $\overline{\text{ERC}}$ signal OFF timer is operating, (3) start is delayed due to operation of direction switchover timer, (4) INP signal is waited for, thereby delaying cessation of pulse output or (5) the PCL5022 is in start/stop sequence. Refer to explanation of bits 11 and 32 of environment setting register 2 (5.6.10).

Interrupt request from 'a' or 'b' axis

If one or more interrupt factors are generated on 'a' or 'b' axis, bit 6 or 7 becomes 0. When no interrupt factor exist, the bit is 1. Refer to "5.4.12 Interrupt Signal Output."

(2) ON/OFF Status of General-purpose I/O Pins

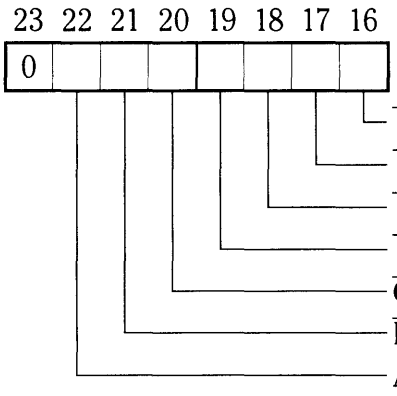
You can read ON/OFF status of general-purpose I/O pins AP0 to AP3 from the address of AP pin monitor (No. 1 with Z80 interface), whether they are defined as input or output.



AP0a pin	0: Low	1: High
AP1a pin	0: Low	1: High
AP2a pin	0: Low	1: High
AP3a pin	0: Low	1: High
AP0b pin	0: Low	1: High
AP1b pin	0: Low	1: High
AP2b pin	0: Low	1: High
AP3b pin	0: Low	1: High

(3) Status of 'a' Axis

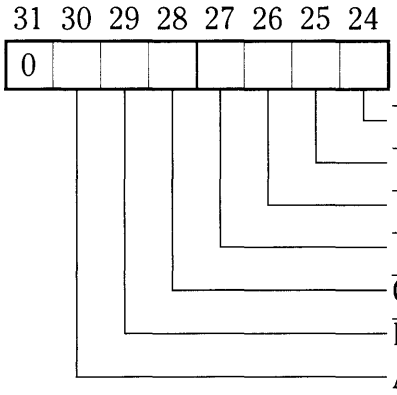
You can read the status of 'a' axis from the address (No. 2 with Z80 interface).



$\overline{+ELa}$ signal	0: OFF	1: ON
$\overline{-ELa}$ signal	0: OFF	1: ON
$\overline{+SDa}$ signal	0: OFF	1: ON
$\overline{-SDa}$ signal	0: OFF	1: ON
$\overline{ORGa}$ signal	0: OFF	1: ON
$\overline{EZa}$ signal	0: OFF	1: ON
ALMa signal	0: OFF	1: ON

(4) Status of 'b' Axis

You can read the status of 'b' axis from the address (No. 3 with Z80 interface).



$\overline{+ELb}$ signal	0: OFF	1: ON
$\overline{-ELb}$ signal	0: OFF	1: ON
$\overline{+SDb}$ signal	0: OFF	1: ON
$\overline{-SDb}$ signal	0: OFF	1: ON
$\overline{ORGb}$ signal	0: OFF	1: ON
$\overline{EZb}$ signal	0: OFF	1: ON
ALMb signal	0: OFF	1: ON

NOTE: $\overline{\pm SD}$ and $\overline{ORG}$ signals are latched.

6. Hardware

6.1 Terminal Pin Assignment

Pin No.	Name	Input/Output	Logic	Description
1	$\overline{RST}$	I	Negative	Reset signal
2	$\overline{INT}$	O*1	Negative	Interrupt signal
3	$\overline{WRQ}$	O	Negative	Wait request signal
4	$\overline{CS}$	I	Negative	Chip select signal
5	$\overline{RD}$ (E)	I	Negative	Read signal
6	$\overline{WR}$ (R/$\overline{W}$)	I	Negative	Write signal
7	$\overline{US}$	I	Negative	High-place data select signal
8	A0 ($\overline{LS}$)	I	Positive	Address bus 0 (low-place data select signal)
9	A1	I	Positive	Address bus 1
10	A2	I	Positive	Address bus 2
11	NC			Unused
12	D0	I/O	Positive	Data bus 0 (LSB)
13	D1	I/O	Positive	Data bus 1
14	D2	I/O	Positive	Data bus 2
15	GND	I		
16	D3	I/O	Positive	Data bus 3
17	D4	I/O	Positive	Data bus 4
18	D5	I/O	Positive	Data bus 5
19	D6	I/O	Positive	Data bus 6
20	D7	I/O	Positive	Data bus 7
21	D8	I/O	Positive	Data bus 8
22	D9	I/O	Positive	Data bus 9
23	D10	I/O	Positive	Data bus 10
24	D11	I/O	Positive	Data bus 11
25	D12	I/O	Positive	Data bus 12
26	D13	I/O	Positive	Data bus 13
27	D14	I/O	Positive	Data bus 14
28	D15	I/O	Positive	Data bus 15
29	+5V	I		
30	ELLa	I*2		$\overline{\pm EL}$ signal input logic, 'a' axis
31	ELLb	I*2		$\overline{\pm EL}$ signal input logic, 'b' axis
32	AP0a	I/O	Positive	General-purpose port, 'a' axis
33	AP1a	I/O	Positive	General-purpose port, 'a' axis
34	AP2a	I/O	Positive	General-purpose port, 'a' axis

Pin No.	Name	Input/Output	Logic	Description
35	AP3a	I/O	Positive	General-purpose port, 'a' axis
36	AP0b	I/O	Positive	General-purpose port, 'b' axis
37	AP1b	I/O	Positive	General-purpose port, 'b' axis
38	AP2b	I/O	Positive	General-purpose port, 'b' axis
39	AP3b	I/O	Positive	General-purpose port, 'b' axis
40	GND	I		
41	+5V	I		
42	$\overline{\text{OUTa}}$	O	Negative*3	Command pulse, 'a' axis
43	DIRa	O	H*3	Direction signal, 'a' axis
44	NC			Unused
45	$\overline{\text{OUTb}}$	O	H*3	Command pulse, 'b' axis
46	DIRb	O	H*3	Direction signal, 'b' axis
47	NC			Unused
48	GND	I		
49	$\overline{+\text{ELa}}$	I*2	Negative*4	End limit signal in plus direction, 'a' axis
50	$\overline{-\text{ELa}}$	I*2	Negative*4	End limit signal in minus direction, 'a' axis
51	$\overline{+\text{SDa}}$	I*2	Negative*3	Ramping-down signal in plus direction, 'a' axis
52	$\overline{-\text{SDa}}$	I*2	Negative*3	Ramping-down signal in minus direction, 'a' axis
53	$\overline{\text{ORGa}}$	I*2	Negative*3	Origin return signal, 'a' axis
54	$\overline{+\text{ELb}}$	I*2	Negative*4	End limit signal in plus direction, 'b' axis
55	$\overline{-\text{ELb}}$	I*2	Negative*4	End limit signal in minus direction, 'b' axis
56	$\overline{+\text{SDb}}$	I*2	Negative*3	Ramping-down signal in plus direction, 'b' axis
57	$\overline{-\text{SDb}}$	I*2	Negative*3	Ramping-down signal in minus direction, 'b' axis
58	$\overline{\text{ORGb}}$	I*2	Negative*3	Origin return signal, 'b' axis
59	$\overline{\text{ALMa}}$	I*2	Negative*3	Alarm signal, 'a' axis
60	$\overline{\text{INPa}}$	I*2	Negative*3	In-position signal, 'a' axis
61	$\overline{\text{ERCa}}$	O*1	Negative	Deviation counter clear signal, 'a' axis
62	$\overline{\text{ALMb}}$	I*2	Negative*3	Alarm signal, 'b' axis
63	$\overline{\text{INPb}}$	I*2	Negative*3	In-position signal, 'b' axis
64	$\overline{\text{ERCb}}$	O*1	Negative	Deviation counter clear signal, 'b' axis
65	$\overline{\text{CLRa}}$	I*2	Negative	Up/down counter clear signal, 'a' axis
66	GND	I		
67	$\overline{\text{CLRb}}$	I*2	Negative	Up/down counter clear signal, 'b' axis

Pin No.	Name	Input/Output	Logic	Description
68	RSs	I*2	Positive	Encoder A signal, 'a' axis
69	EBa	I*2	Positive	Encoder B signal, 'a' axis
70	$\overline{\text{EZa}}$	I*2	Negative*3	Encoder Z signal, 'a' axis
71	ERAa	I*2	Positive	Out-of-step detection encoder A signal, 'a' axis
72	ERBa	I*2	Positive	Out-of-step detection encoder B signal, 'a' axis
73	EAb	I2	Positive	Encoder A signal, 'b' axis
74	EBb	I*2	Positive	Encoder B signal, 'b' axis
75	$\overline{\text{EZb}}$	I*2	Negative*3	Encoder Z signal, 'b' axis
76	ERAb	I*2	Positive	Out-of-step detection encoder A signal, 'b' axis
77	ERBb	I*2	Positive	Out-of-step detection encoder B signal, 'b' axis
78	PAa	I*2	Positive	Pulser A signal, 'a' axis
79	PBa	I*2	Positive	Pulser B signal, 'a' axis
80	PAb	I*2	Positive	Pulse A signal, 'b' axis
81	PBb	I*2	Positive	Pulser B signal, 'b' axis
82	GND	I		
83	$\overline{\text{BSYa}}$	O	Negative	Operation-in-progress signal, 'a' axis
84	$\overline{\text{FUPa}}$	O	Negative	Acceleration-in-progress signal, 'a' axis
85	$\overline{\text{FDWa}}$	O	Negative	Deceleration-in-progress signal, 'a' axis
86	NC			Unused
87	$\overline{\text{BSYb}}$	O	Negative	Operation-in-progress signal, 'b' axis
88	$\overline{\text{FUPb}}$	O	Negative	Acceleration-in-progress signal, 'b' axis
89	$\overline{\text{FDWb}}$	O	Negative	Deceleration-in-progress signal, 'b' axis
90	GND	I		
91	+5V	I		
92	+5V	I		
93	NC			Unused
94	$\overline{\text{STA}}$	I/O*1	Negative	Simultaneous start signal
95	$\overline{\text{STP}}$	I/O*1	Negative	Simultaneous stop signal
96	I/$\overline{\text{M}}$	I		Intel/Motorola interface setting
97	B/$\overline{\text{W}}$	I		8-bit/16-bit interface setting
98	GND	I		
99	CLK	I		Reference clock
100	+5V	I		

Notes:

*1. With pull-up register and connectable in wired OR

*2. With pull-up resistor

*3. The logic is changeable with a software technic and the indicated one is the default logic.

*4. The logic is changeable by setting the pin and the indicated one is the default logic.

"H" in the logic column means that the pin is at high level under the initial condition.

Precautions:

- Do not connect any signal to NC pins.
- Pull-up resistors are mounted to prevent the pins from floating. To pull up signals, connect resistors dedicated to the system.

6.2 Terminal Pin Functions (Pin No. in brackets)

6.2.1 +5V [29, 41, 91, 92, 100], GND [15, 40, 48, 66, 82, 90, 98]

These are power input pins. Be sure to input +5V ±5% to all +5V pins and connect all GND pins to the ground.

6.2.2 NC [11, 44, 47, 86, 93]

NC pins are unused pins. Do not connect any signal to these pins.

6.2.3 I/$\overline{M}$ [96]

This pin determines the CPU interface specification, Intel or Motorola.

6.2.4 B/$\overline{W}$ [97]

This pin determines the CPU interface specification, byte access or word access.

6.2.5 CLK [99]

This pin inputs the reference clock which is used to control the internal circuit. It is recommended to use a reference clock of 9.8304MHz. Output pulses are produced referring to the clock frequency input to this pin. Accordingly, the accuracy of output pulses depends on the reference clock.

6.2.6 $\overline{RST}$ [1]

When the PCL5022 receives more than 8 cycles of the reference clock with this pin at low level, it is reset. For conditions after reset, refer to "4.5 Default (Reset) Conditions of PCL5022."

6.2.7 $\overline{INT}$ [2]

This pin output interupt request signals to the CPU. When using multiple units of PCL5022, you can connect INT pins of all units in wired OR. This pin requires an external pull-up resistor of 5kΩ to 10kΩ. Reading the interrupt factor from the R12 register to the input/output buffer resets the ON status to OFF. The input status can be read through the R15 register.

6.2.8 WRQ [3]

Processing a command requires four cycles at the reference clock. This pin outputs the signal to let the CPU stand by if the CPU tries to access to the PCL5022 durint processing the command. The signal is used as a wait request.

6.2.9 $\overline{\text{RD}}$ (E) [4]

Putting this pin at low level enables RD and WR pins.

6.2.10 $\overline{\text{RD}}$ (E) [5]

The $\overline{\text{CS}}$ pin at low level enables this pin. The pin inputs the $\overline{\text{RD}}$ signal (Intel) or the E signal (8-bit, Motorola).

6.2.11 $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) [6]

The $\overline{\text{CS}}$ pin at low level enables this pin. The pin inputs the $\overline{\text{WR}}$ (Intel) or the R/$\overline{\text{W}}$ signal (Motorola).

6.2.12 $\overline{\text{US}}$ [7]

The $\overline{\text{CS}}$ pin at low level enables this pin. The pin inputs high-place data of 16-bit data bus.

6.2.13 A0 to A2 [8 to 10]

These pins input address signals. With the 16-bit data bus connected, the A0 pin inputs low-place data of 16-bit data bus.

6.2.14 D0 to D7 [12 to 14, 16 to 20]

These pins form a bidirectional data bus. With the 16-bit data bus connected, these pins connect to low-place 8 bits.

6.2.15 D8 to D15 [21 to 28]

With the 16-bit data bus connected, these pins connect to high-place 8 bits. With the 8-bit data bus connected, these pins are not used. When they are not used, pull up them by external resistors of 1kΩ to 100kΩ.

6.2.16 ELLa/b [30/31]

These pins set the $\overline{\pm \text{EL}}$ signal input logic. The low level selects the negative logic and the high level, the positive logic.

6.2.17 AP0 to AP3 a/b [32 to 35/36 to 39]

These pins are general-purpose input/output ports. You can define each individual pin as input or output. You can also let the input to the pin initiate the $\overline{\text{INT}}$ signal.

Connect an external pull-up resistor of 1kΩ to 100kΩ to unused AP pins.

6.2.18 $\overline{\text{OUT}}$a/b [42/45]

These pins output motor control pulses. In the common pulse mode, these pins output pulses and the direction depends on the DIR signal. In the 2-pulse mode, these pins output pulses in plus direction. The output logic can be

changed with a software technic and the pulse output can be masked.

6.2.19 DIRa/b [43/46]

These pins output motor control pulses or direction signals. Selection of motor control pulses or direction signals is made in combination with the $\overline{\text{OUT}}$ pin. In the common pulse mode, these pins output direction signals. In the 2-pulse mode, these pins output pulses in minus direction. The output logic can be changed with a software technic and the output in the 2-pulse mode can be masked.

6.2.20 $\overline{+\text{EL}}$ab [49/54], $\overline{-\text{EL}}$a/b [50/55]

These pins input end limit signals in plus and minus directions, respectively. The input logic can be changed with the ELL pin and the input status can be monitored by reading the status code.

6.2.21 $\overline{+\text{SD}}$a/b [51/56], $\overline{-\text{SD}}$a/b [52/57] [63] with Pull-up Resistor

These pins input ramping-down signals in plus and minus directions, respectively. The input logic can be changed with a software technic and the input can be masked. The input status can be monitored by reading the status code or by reading the R15 register.

6.2.22 $\overline{\text{ORG}}$a/b [53/58] with Pull-up Resistor

These pins input the origin signal. The input logic can be changed with a software technic. The input status can be monitored by reading the status code or reading the R15 register.

6.2.23 $\overline{\text{ALM}}$a/b [59/62] with Pull-up Resistor

These pins input external alarm signals. The PCL5022 stops outputting pulses immediately receiving an alarm at the $\overline{\text{ALM}}$ pin. If you write the start command with the $\overline{\text{ALM}}$ pin ON, the PCL5022 does not output any pulse. The input logic can be changed with a software technic. The input status can be monitored by reading the status code.

6.2.24 $\overline{\text{INP}}$a/b [60/63] with Pull-up Resistor

These pins input the in-position signal from the servo driver. The input logic can be changed with a software technic. The input status can be monitored by reading the R15 register.

6.2.25 $\overline{\text{ERC}}$a/b [461/64]

These pins output the signal to reset the deviation counter of servo driver. The pulsewidth of output signal is 4096 cycles at the reference clock (approximately 400μ with a reference clock of 9.8304MHz). The output status can be monitored by reading the R15 register. These pins require an external pull-up resistor of 5kΩ to 10kΩ. If you do not these pins, place them in an open condition.

6.2.26 $\overline{\text{CLR}}$a/b [65/67] with Pull-up Resistor

The CLR pin changing from high to low level resets the up/down counter of the axis. (The up/down counter counts with the pin at low level.) You can let the $\overline{\text{INT}}$ signal be output when the up/down counter is reset. The high/low status can be monitored by reading the R15 register.

6.2.27 EAa/b [68/73], EBa/b [69/74] with Pull-up Resistor

Use these pins when you want to let the up/down counter count encoder signals. You can let these pins input 1x, 2x or 4x 90° phase difference signals or the EA pin input plus pulses and the EB pin input minus pulses. With 90° phase difference signals, the up/down counter count up when the phase of EA signal advance over the EB signal.

6.2.28 $\overline{\text{EZ}}$a/b [70/75] with Pull-up Resistor

These pins input a marker signal the encoder outputs at every revolution. The EZ signal improves the accuracy of origin return. The input logic can be changed with a software technic. The input status can be monitored by reading the status code.

6.2.29 ERAa/b [71/76], ERBa/b [72/77] with Pull-up Resistor

These pins input signals from the encoder for out-of-step detection. You can let these pins input 1x, 2x or 4x 90° phase difference signals or the ERA pin input plus pulses and the ERB pin input minus pulses. With 90° phase difference signals, input signals in such a manner that the phase of ERA signal advances over the ERB signal in operation in plus direction.

6.2.30 PAa/b [78/80], PBa/b [79/81] with Pull-up Resistor

These pins input external pulse signals. In the continuous mode 2 or the preset mode 2, external pulse signals input to these pins let the PCL5022 output pulses from $\overline{\text{OUT}}$ and DIR pins. Moving direction in the continuous mode 2 is judged based on PA and PB signals. In the preset mode 2, the moving direction is as set by the CPU. You can let these pins input 1x, 2x or 4x 90° phase difference signals or the PA pin input plus pulses and the PB pin input minus pulses. With 90° phase difference signals, the moving direction is plus when the phase of PA signal advances over the PB signal. You can use these pins to input pulser (manual rotation encoder) signals.

6.2.31 $\overline{\text{BSY}}$a/b [83/87]

These pins are low level when the PCL5022 is outputting pulses. The$\overline{\text{INP}}$ signal delays the output timing. The output status can be monitored by reading the R15 register.

6.2.32 $\overline{\text{FU}}$Pa/b [84/88]

These pins are low level when the PCL5022 ramps down the pulse output.

6.2.33 $\overline{\text{FDW}}$a/b [85/89]

These pins are low level when the PCL5022 ramps down the pulse output.

6.2.34 $\overline{\text{STA}}$a/b [94]

If you use two or more units of PCL5022 to control multiple axes, connect the $\overline{\text{STA}}$ pins of all units, and the $\overline{\text{STA}}$ signal will simultaneously start all axes. Writing the simultaneous start command lets this pin output pulse signal with a width of 512 cycles at the reference clock (approximately 52μs with a reference clock of 9.8304MHz). If connected to such the effect, you can staart a specific axis only with a software technic. Simultaneous start of multiple axes is also available with an external signal. The pin status can be monitored by reading the R15 register.

If you do not use the pin, place it in an open condition.

6.2.35 $\overline{\text{STP}}$a/b [95]

If you use two or more units of PCL5022, connect the $\overline{\text{STP}}$ pins of all units. All units will simultaneously stop outputting pulses if some unit stops generating pulses due to an abnormal event. You can select the way of simultaneous stop from immediate stop and deceleration-step. The factor to initiate the simultaneous stop or the simultaneous stop command lets this pin output a pulse signal with a width of 512 cycles at the reference clock (approximately 52μs with a reference clock of 9.8304MHz). If connect to such an effect, you can let the PCL5022 output pulses when the $\overline{\text{STP}}$ pin outputs the signal. Simultaneous stop of multiple axes is also available with an external signal.

When this pin is low level, the start command does not start the PCL5022. The pin status can be monitored by reading the R15 register.

If you do use this pin, place it in an open condition.

6.3 CPU Interface Function

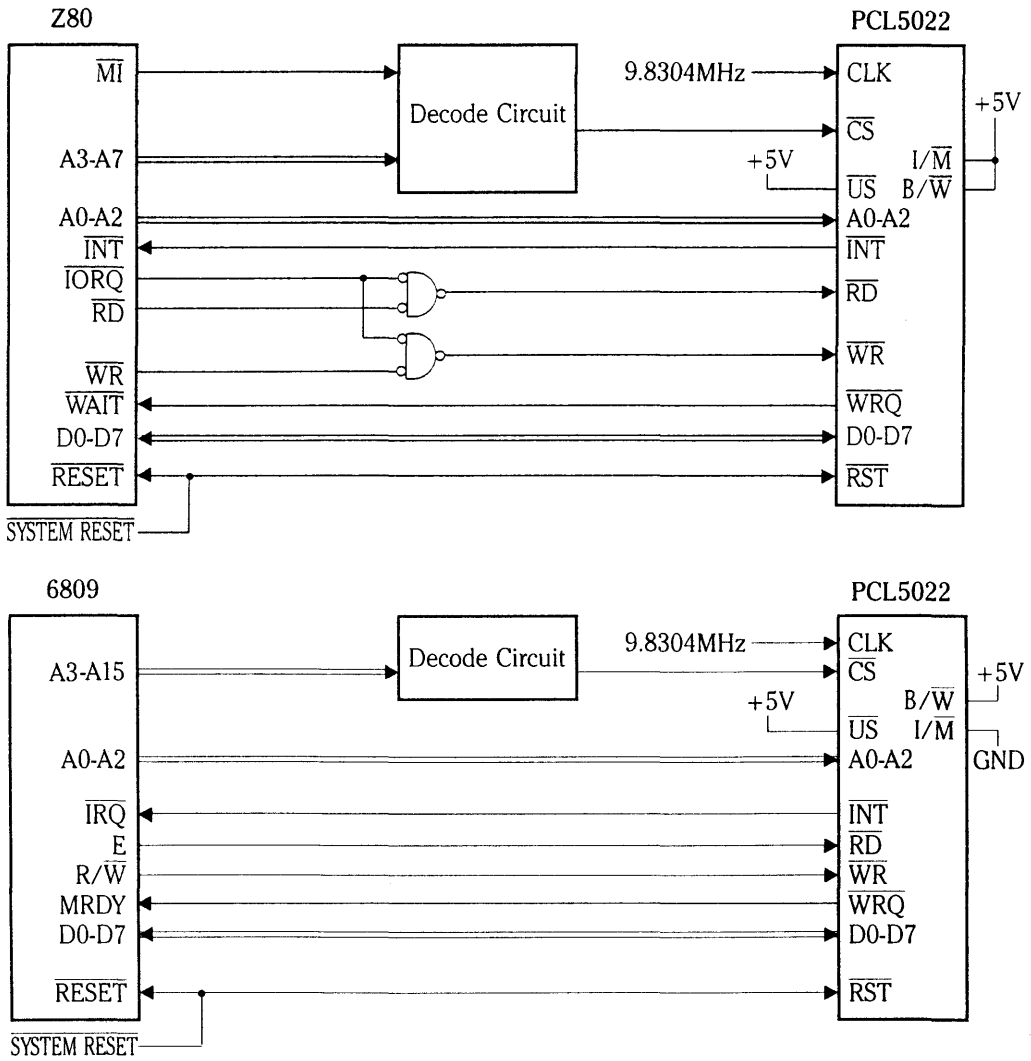
The PCL5022 is so designed that you can connect it to the Intel or Motorola CPU of 8 or 16 bits by setting I/$\overline{M}$ and B/$\overline{W}$ pins as follows.

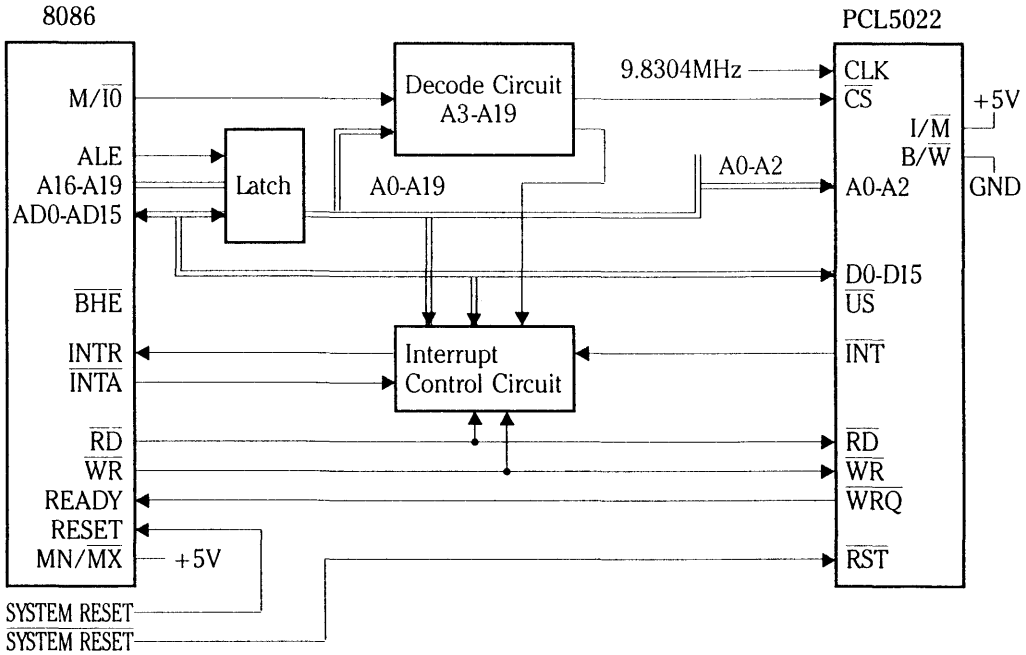
CPU	I/$\overline{M}$ Pin	B/$\overline{W}$ Pin	Interface Specifications
6809	L	H	Motorola 8-bit CPU
8086	H	L	Intel 16-bit CPU
Z80	H	H	Intel 8-bit CPU
	L	L	Prohibited setting

Connect CPU signals as follows.

CPU	Terminal Pins on PCL5022						
	$\overline{RD}$	$\overline{WR}$	A2	A1	A0	$\overline{US}$	$\overline{WRQ}$
8086	$\overline{RD}$	$\overline{WR}$	A2	A1	A0	$\overline{BHE}$	READY
Z80	$\overline{RD}$	$\overline{WR}$	A2	A1	A0	+5V	$\overline{WAIT}$
6809	E	E/$\overline{W}$	A2	A1	A0	+5V	MRDY

6.4 Block Diagrams of CPU Interface Circuit





6.5 Precautions in Designing Hardware

- Notice that the CLK pin only operates at the CMOS level.
- Allow a time length of over eight cycles at the reference clock for the $\overline{RST}$ signal at low level.
- Using a resistor of 1kΩ to 100kΩ, pull up any of pins AP0 to AP2 which will not be used.
- If you connect the PCL5022 to the CPU via the 8-bit bus, pull up pins 8 to 15 using resistors of 1kΩ to 100kΩ.
- If you connect the PCL5022 to the CPU via the 8-bit bus, connect the $\overline{US}$ pin to +5V.
- For safety the input logic of $\overline{+EL}$ and $\overline{-EL}$ pins cannot be changed with a software technic. If you need to change the input logic, use the ELL pin.
- Though $\overline{INT}$ and $\overline{ERC}$ pins have a pull-up resistor built in, you need to additionally mount an external pull-up resistor of 5kΩ to 10kΩ, since their resistance is high.

7. Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Voltage	V_{dd}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to V_{dd} +0.3	V
Input Current	I_{IN}	±10	mA
Storage Temperature	T_{stg}	−40 to +125	°C

7.2 Recommended Operating Conditions

Item	Symbol	Rating	Unit
Power Voltage	V_{dd}	4.75 to 5.25	V
Ambient Temperature	T_J	0 to +70	°C

7.3 DC Characteristics

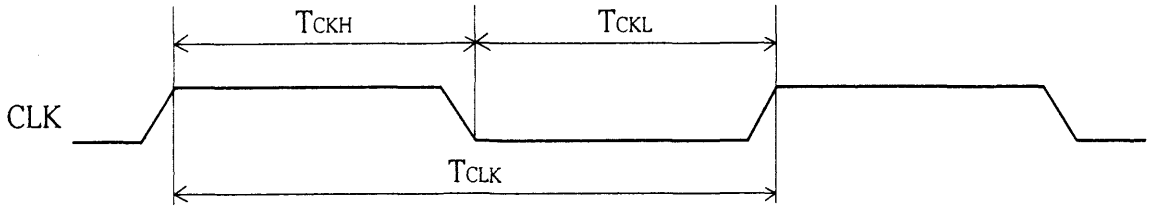
Item	Symbol	Condition	Min.	Max.	Unit
Static Current Consumption	I_{dd1}	CLK = 0Hz		100	μA
Current Consumption	I_{dd2}	Note 1		40	mA
Output Leakage Current	I_{OZ}	Note 2	−10	10	μA
		Note 3	−200	10	μA
Input Capacity				2.3	pF
Low Level Input Current	I_{IL}	Note 4	−10	10	μA
		Note 5	−200	−10	μA
High Level Input Current	I_{IH}		−10	10	μA
Low Level Input Voltage	V_{IL}	Note 6		0.8	V
		Note 7		1.0	V
High Level Input Voltage	V_{IH}	Note 6	2.2		V
		Note 7	4.0		V
Low Level Output Voltage	V_{OL}	I_{OL} = 1μA		0.05	V
		I_{OL} = 8mA		0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = −1μA	V_{dd} − 0.05		V
		I_{OH} = −8mA	2.4		V
Internal Pull-up Resistance	R_{UP}		25	500	kΩ

NOTES: 1. CLK = 9.8304MHz, output frequency = 1.22865MHz, with no load
2. D0–D15, AP0–AP3, $\overline{OUT}$, DIR, $\overline{BSY}$, $\overline{FUP}$, $\overline{FDW}$
3. $\overline{ERC}$, $\overline{STA}$, $\overline{STP}$, $\overline{INT}$, $\overline{WRQ}$
4. $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{US}$, A0–A2, D0–D15, CLK, $\overline{RST}$
5. $\overline{CLR}$, EA, EB, $\overline{EZ}$, PA, PB, ERA, ERB, $\overline{ALM}$, $\overline{INP}$, $\overline{ERC}$, $\overline{+EL}$, $\overline{-EL}$, $\overline{+SD}$, $\overline{-SD}$, $\overline{ORG}$, $\overline{STA}$, $\overline{STP}$, I/$\overline{M}$, B/$\overline{W}$, ELL
6. Input of other than CLK and input/output pins
7. CLK pin only

7.4 AC Characteristics

7.4.1 Reference Clock

Item	Symbol	Condition	Min.	Max.	Unit
Reference Clock Frequency	f_{CLK}			10	MHz
Cycle Time at Reference Clock	T_{CLK}		100		ns
Time Width of High Level	T_{CKH}		40		ns
Time Width of Low Level	T_{CKL}		40		ns

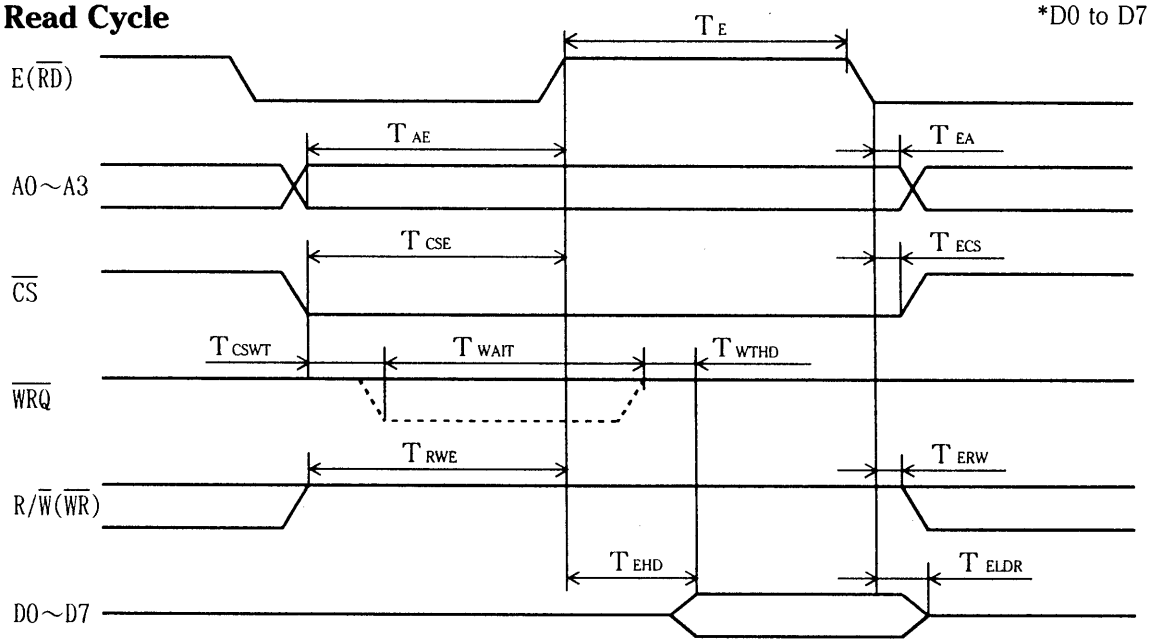


7.4.2 CPU Interface 1 (I/$\overline{M}$=L, B/$\overline{W}$=H) to 6809

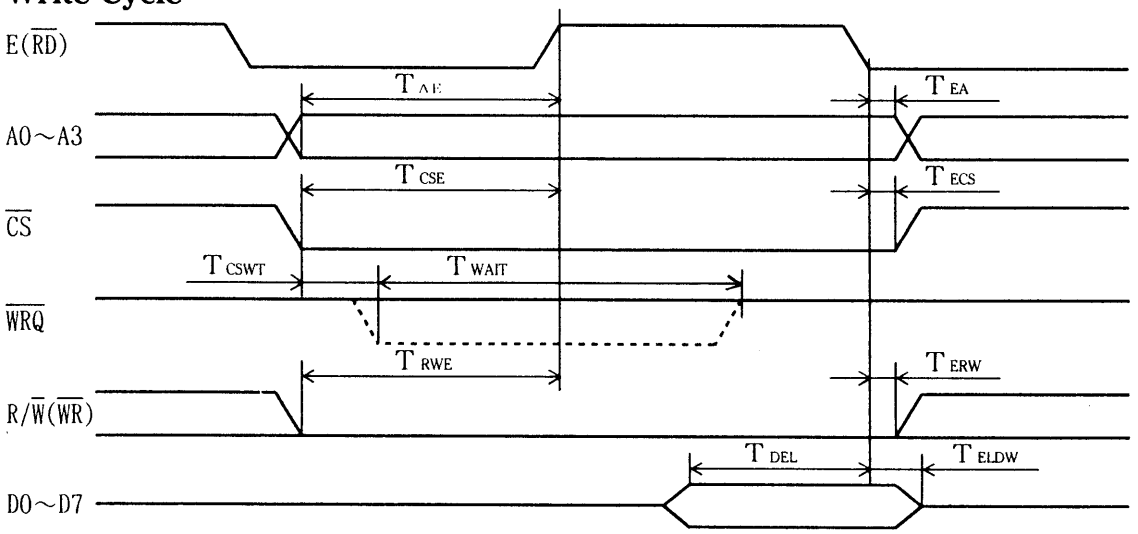
Item		Symbol	Condition	Min.	Max.	Unit
E Signal High Level Time		T_E	C_L=85pF*	45		ns
Address Setup Time	to E ↑	T_{AE}		7		ns
Address Hold Time	to $\overline{E}$ ↓	T_{EA}		0		ns
CS Setup Time	to E ↑	T_{CSS}		3		ns
CS Hold Time	to E ↓	T_{ECS}		0		ns
$\overline{WRQ}$ Delay Time	to CS ↓	T_{CSWT}	C_L=85pF		32	ns
$\overline{WRQ}$ Signal Low Level Time		T_{WAI}			4·T_{CLK}	ns
R/$\overline{W}$ Setup Time	to E ↑	T_{RWE}		7		ns
R/$\overline{W}$ Hold Time	to ↓	T_{ERW}		4		ns
Data Output Delay Time	to E ↑	T_{EHD}	C_L=85pF		45	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHF}	C_L=85pF		22	ns
Data Float Delay Time	to E ↓	T_{ELDR}	C_L=85pF		37	ns
Data Setup Time	to E ↑	T_{DEL}		9		ns
Data Hold Time	to E ↓	T_{ELDW}		0		ns

*D0 to D7

Read Cycle



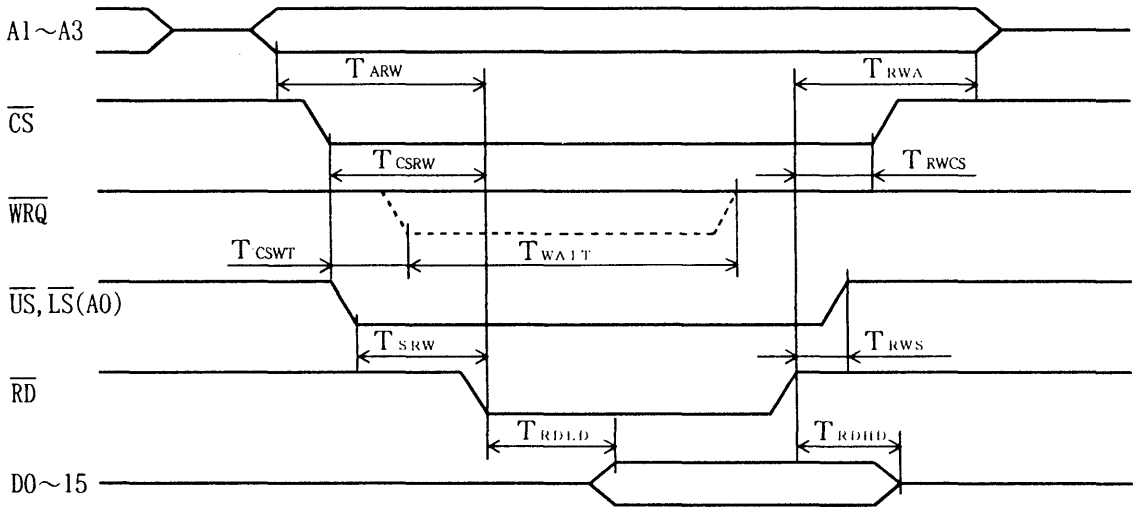
Write Cycle



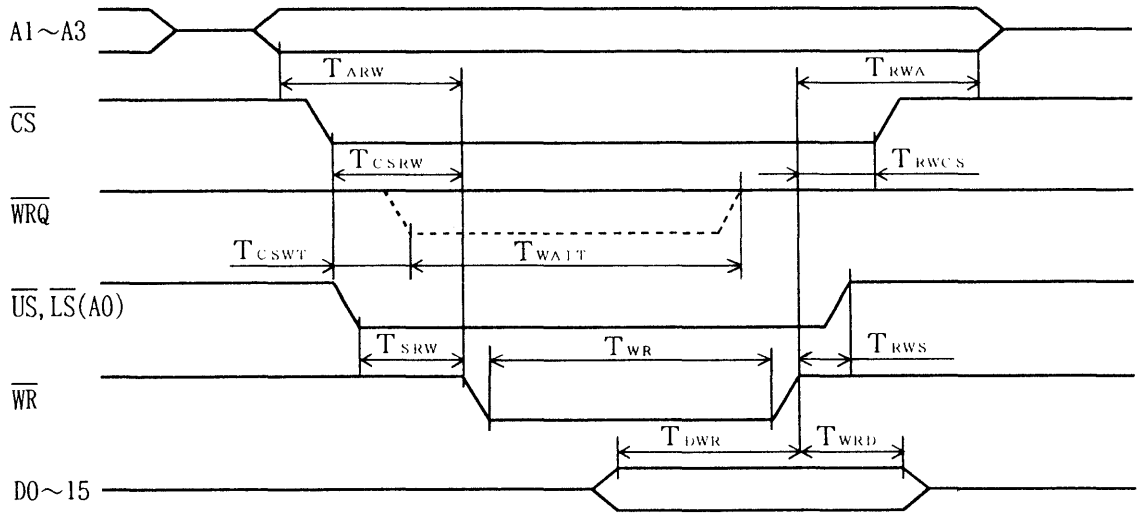
7.4.3 CPU Interface 2 (I/$\overline{M}$=H, B/$\overline{W}$=L) to 8086

Item		Symbol	Condition	Min.	Max.	Unit
Address Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{ARW}		12		ns
Address Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWA}		0		ns
$\overline{CS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{CSRW}		5		ns
$\overline{CS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWCS}		0		ns
$\overline{WRQ}$ ON Delay Time	to $\overline{CS}$ ↓	T_{CSWT}	C_L=85pF		32	ns
Time Length of $\overline{WRQ}$ Signal at Low Level		T_{WAIT}			4·T_{CLK}	ns
$\overline{US}$, $\overline{LS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{SRW}		3		ns
$\overline{US}$, $\overline{LS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWS}		0		ns
Data Output Delay Time	to $\overline{RD}$ ↓	T_{RDLD}	C_L=85pF		50	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHD}	C_L=85pF		22	ns
Data Float Delay Time	to $\overline{RD}$ ↑	T_{RDHD}	C_L=85pF		31	ns
$\overline{WR}$ Signal Width		T_{WR}		8		ns
Data Setup Time	to $\overline{WR}$ ↓	T_{DWR}		16		ns
Data Hold Time	to $\overline{WR}$ ↑	T_{WRD}		0		ns

Read Cycle



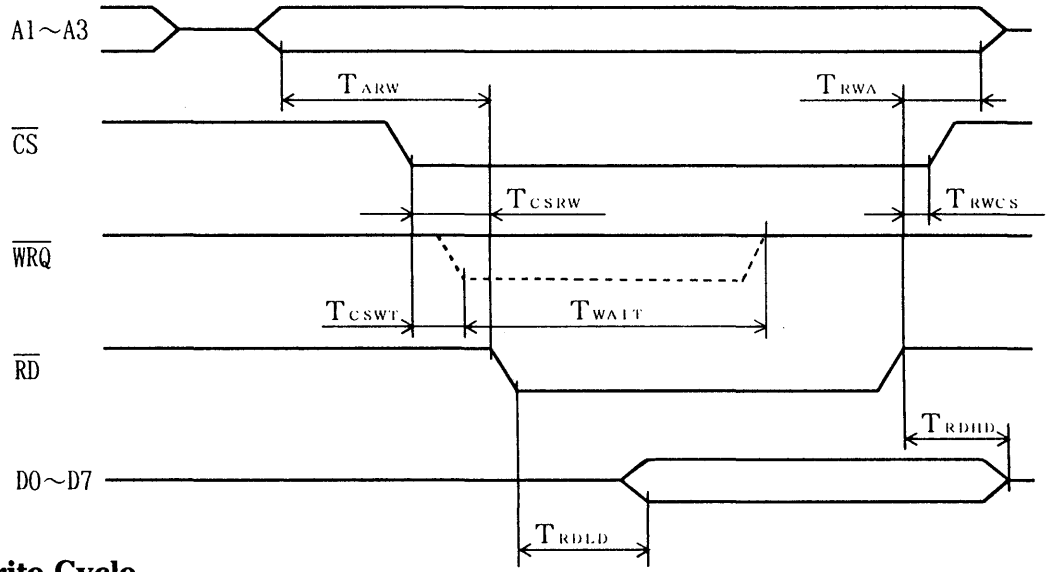
Write Cycle



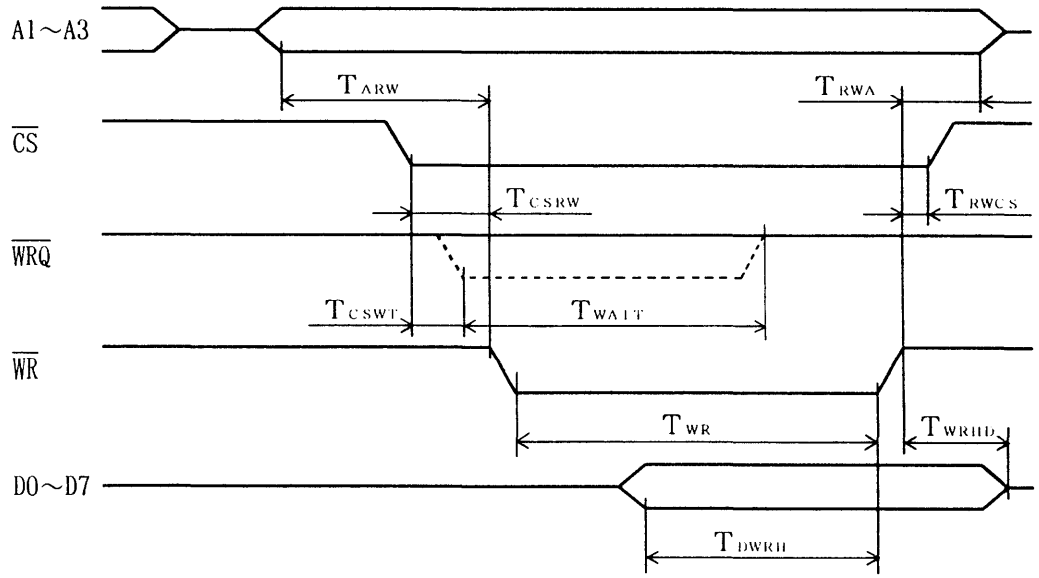
7.4.4 CPU Interface 3 (I/$\overline{M}$=H, B/$\overline{W}$=H) to Z80

Item		Symbol	Condition	Min.	Max.	Unit
Address Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{ARW}		12		ns
Address Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWA}		0		ns
$\overline{CS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{CSRW}		5		ns
$\overline{CS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWCS}		0		ns
$\overline{WRQ}$ ON Delay Time	to $\overline{CS}$ ↓	T_{CSWT}	C_L=85pF		32	ns
Time Length of $\overline{WRQ}$ Signal at Low Level		T_{WAIT}			4·T_{CLK}	ns
Data Output Delay Time	to $\overline{RD}$ ↓	T_{RDLD}	C_L=85pF		50	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHD}	C_L=85pF		22	ns
Data Float Delay Time	to $\overline{RD}$ ↑	T_{RDHD}	C_L=85pF		28	ns
$\overline{WR}$ Signal Width		T_{WR}		8		ns
Data Setup Time	to $\overline{WR}$ ↑	T_{DWRH}		16		ns
Data Hold Time	to $\overline{WR}$ ↑	T_{WRHD}		0		ns

Read Cycle



Write Cycle



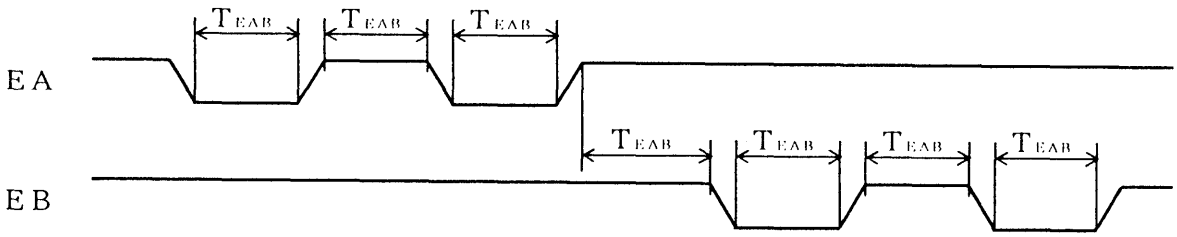
7.4.5 Operation Timing

Item	Symbol	Condition	Min.	Max.	Unit
Time Width of Input $\overline{RST}$ Signal		Note 1	8·T_{CLK}		ns
Time Width of Input $\overline{CLR}$ Signal			2·T_{CLK}		ns
Time Width of Input EA and EB Signals	T_{EAB}		2·T_{CLK}		ns
Time Width of Input $\overline{EZ}$ Signal			2·T_{CLK}		ns
Time Width of Input PA and PB Signals	T_{PAB}		2·T_{CLK}		ns
Time Width of Input ERA and ERB Signals	T_{ERAB}		2·T_{CLK}		ns
Time Width of Input $\overline{ALM}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{INP}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{ERC}$ Signal			4096·T_{CLK}		ns
Time Width of Input $\overline{\pm EL}$ Signals		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{\pm SD}$ Signals		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{ORG}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Output $\overline{STA}$ and $\overline{STP}$ Signals			512·T_{CLK}		ns
Time Width of Input $\overline{STA}$ and $\overline{STP}$ Signals			8·T_{CLK}		ns
$\overline{BSY}$ Signal ON Delay Time	T_{CMDBSY}		5·T_{CLK}	7·T_{CLK}	ns
	T_{STABSY}		11·T_{CLK}	13·T_{CLK}	ns
Start Delay Time	T_{CMDPLS}		21·T_{CLK}	23·T_{CLK}	ns
	T_{STAPLS}		27·T_{CLK}	29·T_{CLK}	ns
$\overline{OUT}$ Signal ON Delay Time	$T_{ON\ OUT}$	C_L=85pF		39	ns
$\overline{OUT}$ Signal OFF Delay Time	$T_{OF\ OUT}$	C_L=85pF		23	ns
DIR Signal HL Delay Time	$T_{HL\ DIR}$	C_L=85pF		54	ns
DIR Signal LH Delay Time	$T_{LH\ DIR}$	C_L=85pF		49	ns
$\overline{BSY}$ Signal ON Delay Time	$T_{ON\ BSY}$	C_L=85pF		35	ns
$\overline{BSY}$ Signal OFF Delay Time	$T_{OF\ BSY}$	C_L=85pF		31	ns
$\overline{FUP}$ Signal ON Delay Time	$T_{ON\ FUP}$	C_L=85pF		40	ns
$\overline{FUP}$ Signal OFF Delay Time	$T_{OF\ FUP}$	C_L=85pF		33	ns
$\overline{FWD}$ Signal ON Delay Time	$T_{ON\ FDW}$	C_L=85pF		41	ns
$\overline{FDW}$ Signal OFF Delay Time	$T_{OF\ FDW}$	C_L=85pF		50	ns
$\overline{STA}$ Signal ON Delay Time	$T_{ON\ STA}$	C_L=85pF		23	ns
$\overline{STA}$ Signal OFF Delay Time	$T_{OF\ STA}$	C_L=85pF		25	ns
$\overline{STP}$ Signal ON Delay Time	$T_{ON\ STP}$	C_L=85pF		51	ns
$\overline{STP}$ Signal OFF Delay Time	$T_{OF\ STP}$	C_L=85pF		25	ns
$\overline{ERC}$ Signal ON Delay Time	$T_{ON\ ERC}$	C_L=85pF		50	ns
$\overline{ERC}$ Signal OFF Delay Time	$T_{OF\ ERC}$	C_L=85pF		25	ns
$\overline{INT}$ Signal ON Delay Time 1	$T_{ON\ IT1}$	C_L=85pF*3		52	ns
$\overline{INT}$ Signal ON Delay Time 2	$T_{ON\ IT2}$	C_L=85pF*4		41	ns
$\overline{INT}$ Signal OFF Delay Time	$T_{OF\ INT}$	C_L=85pF		40	ns

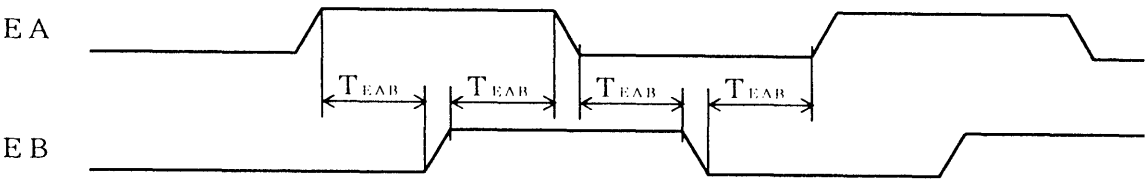
NOTES: 1. Eight cycles of CLK signal should be input during the time the $\overline{RST}$ pin is at low level.

2. The time between 64·T_{CLK} and 48·T_{CLK} is unfixed. Setting bit 8 of R9 at 1 makes a minimum time 2·T_{CLK}.
3. In the case the $\overline{INT}$ signal is output due to a cause other than a signal input to AP0-AP3, ramping-up completed or ramping-down started.
4. In the case the $\overline{INT}$ signal is output due to a signal input to AP0-AP3, ramping-up completed or ramping-down started.

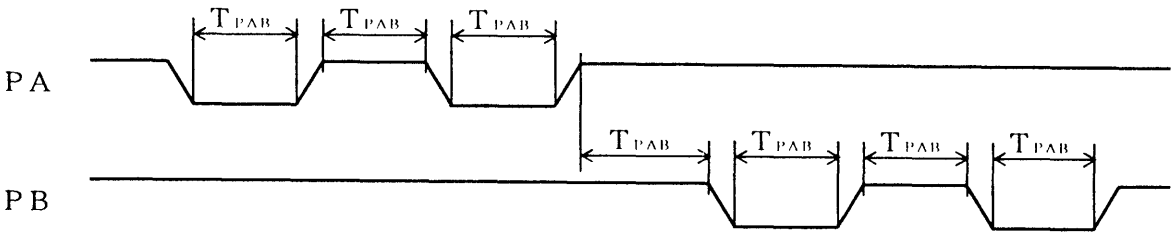
(1) EA and EB Input in 2-pulse Mode



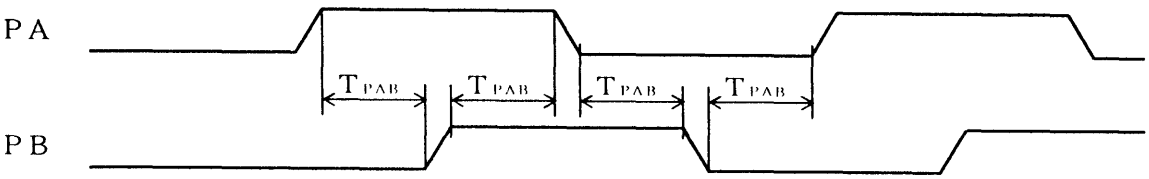
(2) EA and EB Input in 90° Phase Difference Mode



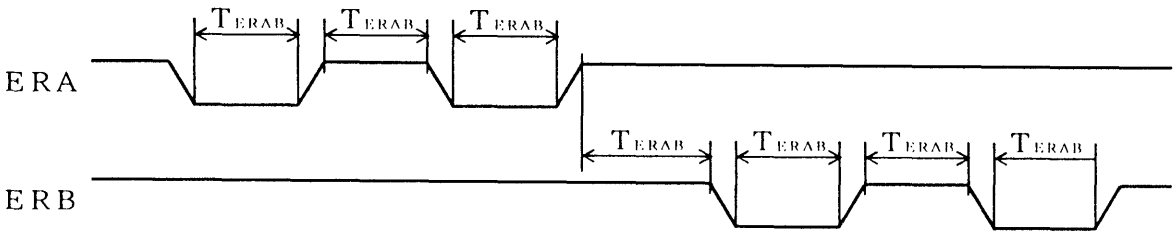
(3) PA and PB Input in 2-pulse Mode



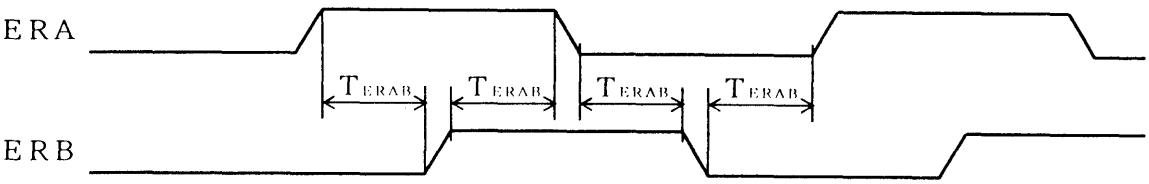
(4) PA and PB Input in 90° Phase Difference Mode



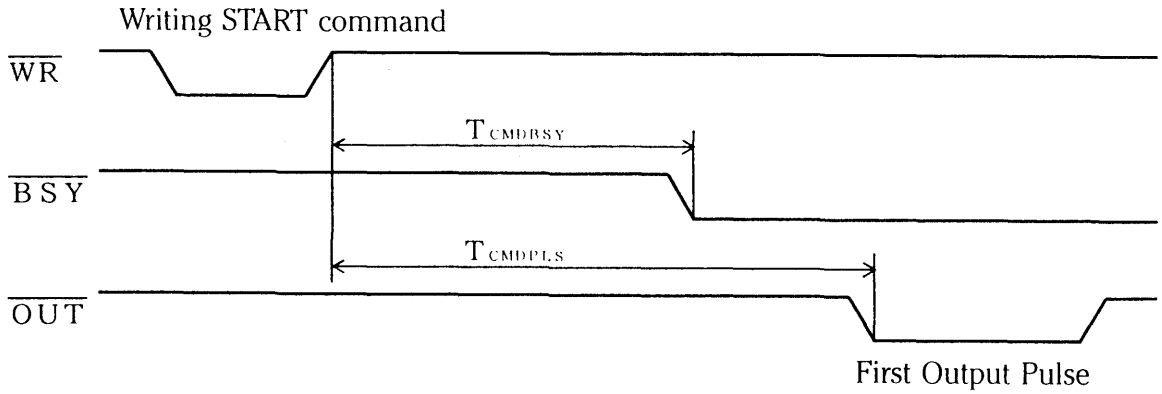
(5) ERA and ERB Input in 2-pulse Mode



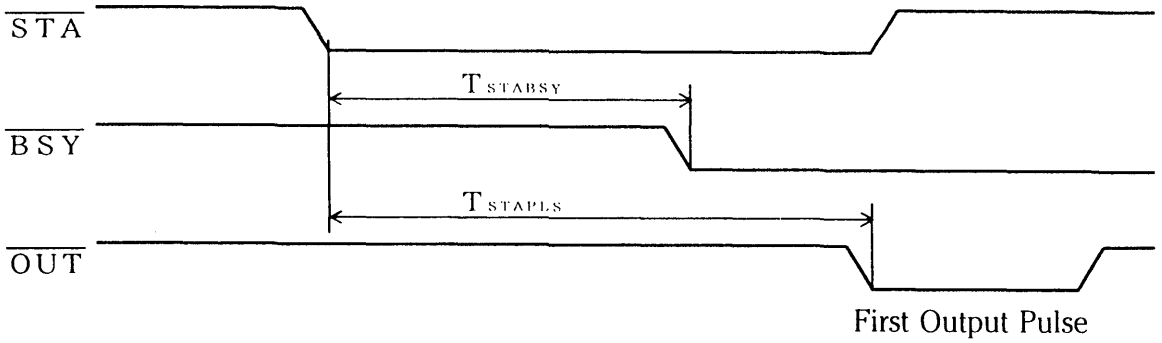
(6) ERA and ERB Input in 90° Phase Difference Mode



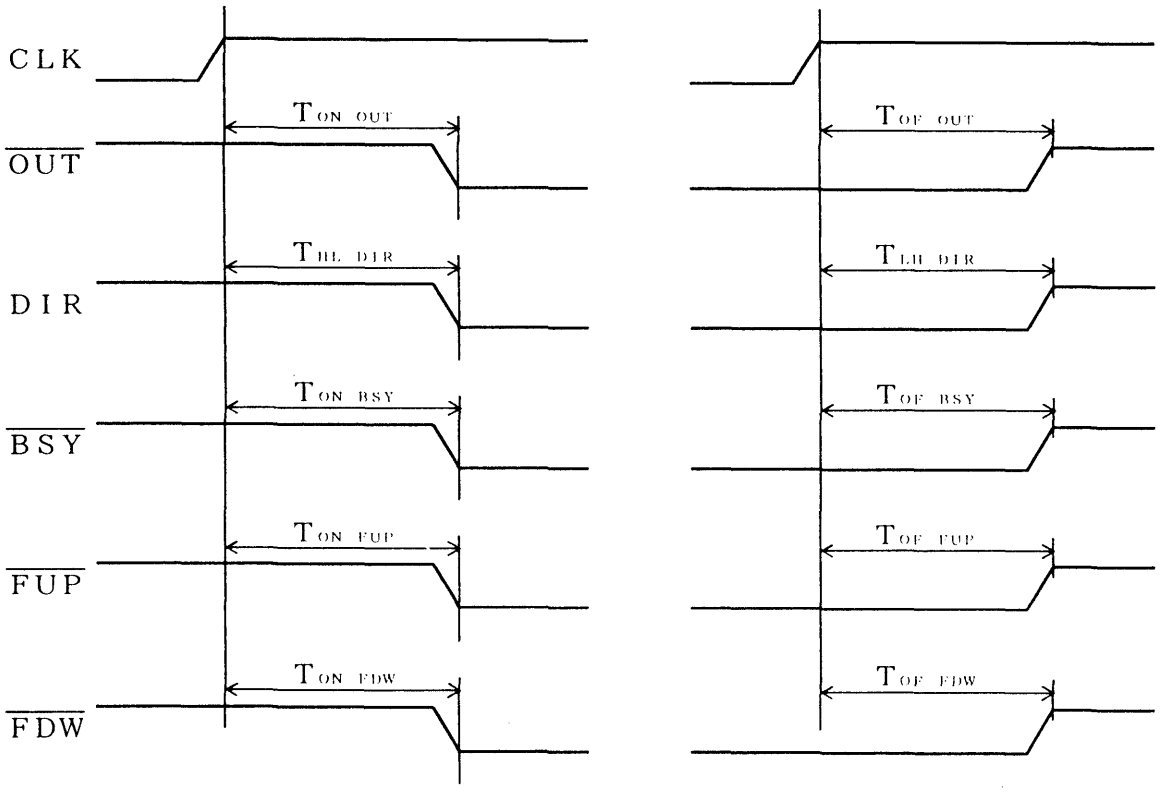
(7) Command Start Timing with I/$\overline{M}$=H and B/$\overline{W}$=H

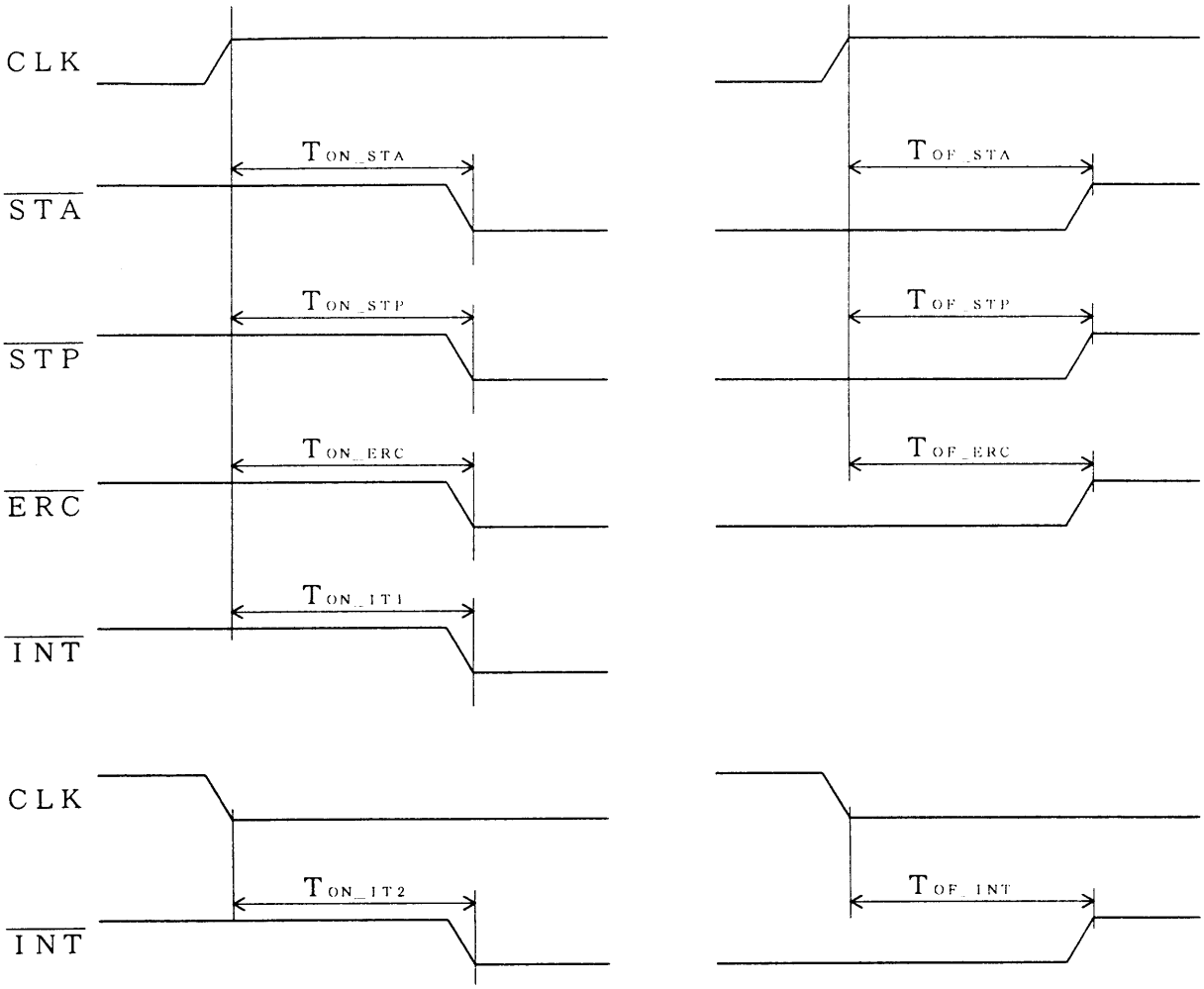


(8) Simultaneous Start Timing



(9) OUT Signal Delay Time




CLK
TON_STA
STA
TON_STP
STP
TON_ERC
ERC
TON_IT1
INT
TOF_STA
TOF_STP
TOF_ERC

CLK
TON_IT2
INT
TOF_INT

8. Handling Precautions

8.1 Designing Precautions

(1) In any case the PCL5022 shall not be subjected to a condition exceeding the absolute maximum ratings.

(2) Protect the PCL5022 from receiving a heating effect from environment and keep ambient temperatures as lowest possible.

(3) A latch-up condition may cause heat generation and fuming. Take the following precautions:

- Do not make the voltage level of input/output pins higher than Vdd and lower than GND. Also, take the power-up timing into consideration.
- Do not apply abnormal noise to the PCL5022.
- Fix the potential of unused input/output pins to Vdd or GND.
- Do not short-circuit the output.
- Protect the PCL5022 against induction and static electricity from a high-voltage generation circuit.

(4) Take care that an excess voltage due to noise, surge and static electricity is not applied to the PCL5022.

8.2 Transportation and Storage Precautions

(1) Handle the packaging gently. Throwing or dropping it may damage the PCL5022 in it.

(2) Do not store the packaging where it may be splashed with water or exposed to direct sunlight.

(3) Do not store the packaging where poisonous or corrosive gases are generated.

(4) Prepare an anti-static container and take care that the PCL5022 may not receive any load.

8.3 Assembling Precautions

(1) Take the following precautions to protect the PCL5022 against damage due to static electricity:

- Ground the instruments and fixtures which are installed at the assembling area.
- Ground the worktable with a conductive mat or the like having resistance. Avoid the metal surface which causes an abrupt electrical discharge with low resistance if an electrified PCL5022 contacts with the surface.
- When picking up the PCL5022 with vacuum, mount a conductive rubber or the like onto the tip of pickup to prevent the PCL5022 from being electrified. Also, use contacts featuring highest possible resistance for connection to lead terminals of PCL5022.

- Tweezers which may contact with pins of PCL5022 should be resistant against static electricity. Avoid metal tweezers if possible. Such tweezers may electrify the PCL5022 through friction and cause electrical discharge.

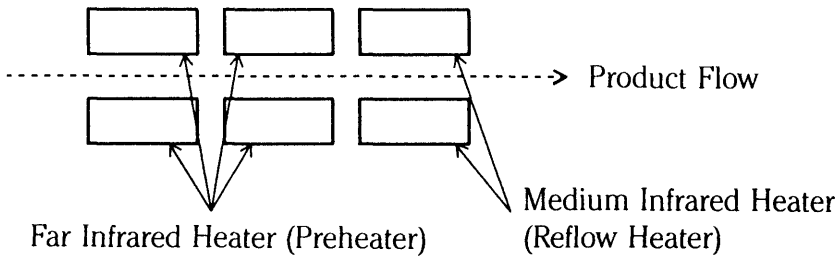
(2) The worker should wear a wrist strap, which should be grounded via 1MΩ resistor.

(3) Use a low-voltage soldering iron and ground it at the tip.

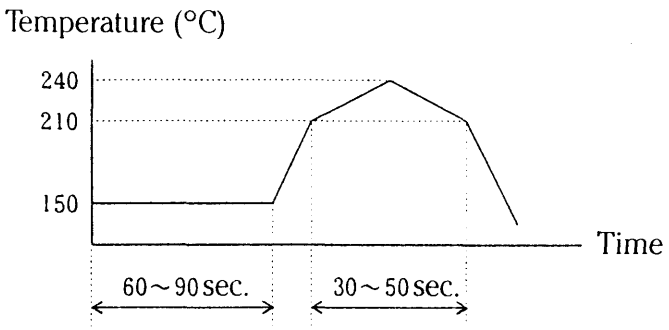
(4) Do not place the PCL5022 or the container near instruments, such as CRT, which generate a high electrical field.

(5) If the fully heating soldering method is used, conduct high-temperature dehumidifying treatment at 125°C for 20 hours.

(6) If soldering is made through an infrared reflow method for reduction of heat stress, the far and medium infrared reflow method is recommended.

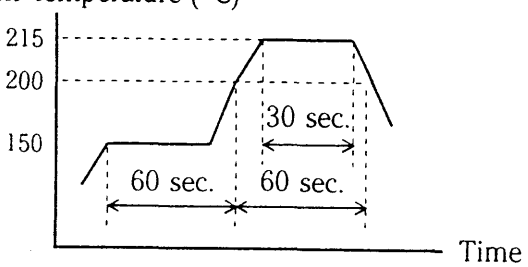


Soldering should be done in such a manner that the time length the package surface and PC board surface are heated to a range of 210°C to 240°C maximum is less than 30 seconds.



(7) For the warm-air reflow, use the same procedure as the far infrared method.

(8) For the vapor phase soldering, Florinade FC-704 or the equivalent is recommended as the solution. Time lengths of heating should be within 30 seconds at 215°C and within 60 seconds at 200°C.



(9) In the case of soldering iron, soldering should be done within 10 seconds at maximum 260°C or within 3 seconds at maximum 350°C.

8.4 Other Precautions

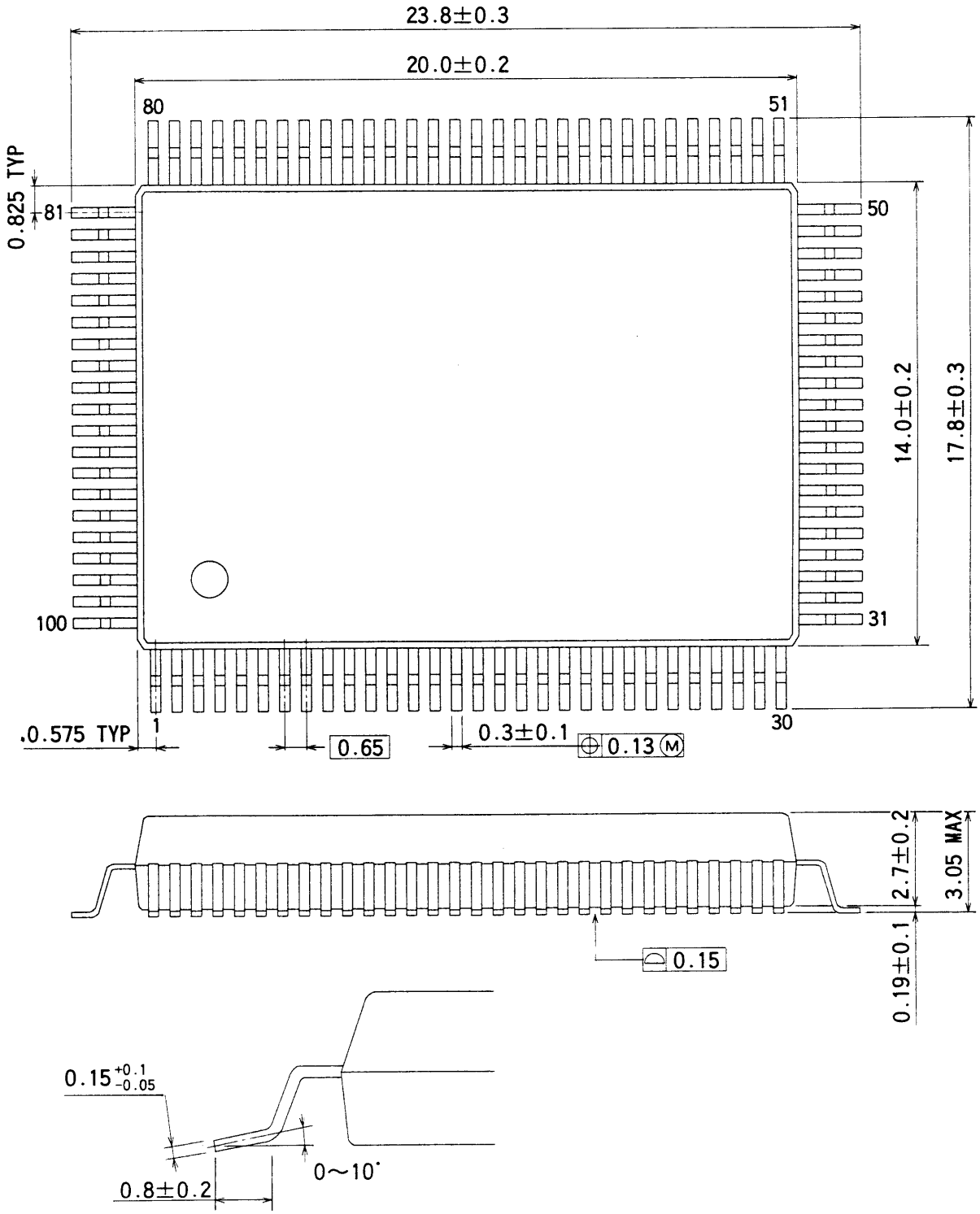
(1) If the PCL5022 is intended for use under adverse environmental conditions (humidity, corrosive gases or dirt), take proper measures such as humidity-resistant coating.

(2) Resin materials used for the package are flame-retardant but not non-inflammable. So it may be burned or fume. Avoid placing it near an inflammable material.

(3) The PCL5022 is designed for office appliances, communications equipment, measuring instruments and home electric appliances. If you use it for the system of which a trouble or erroneous operation may lead to the death or injure the operator, such as nuclear control system, space ship, traffic signal, combustion control system or safety device, take sufficient care.

9. External Dimensions

Unit: mm



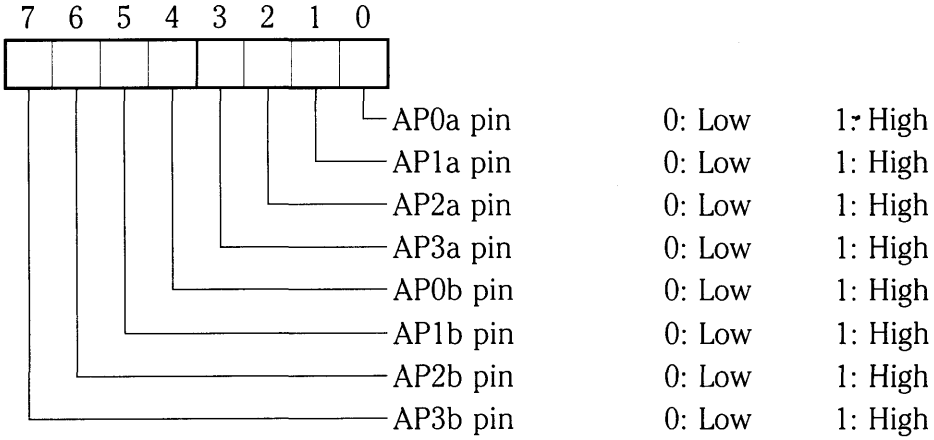
10. Appendix

10.1 List of Commands

10.1.1 Operation Commands (to Address 0 of Z80 Interface)

Commands			Description
a axis	b axis	a/b axes	
00HEX	80HEX	40HEX	Immediately swith to FL pulse rate.
01HEX	81HEX	41HEX	Immediately switch to FH pulse rate.
02HEX	82HEX	41HEX	Decelerate to FL pulse rate.
03HEX	83HEX	43HEX	Accelerate to FH pulse rate.
09HEX	89HEX	49HEX	Immediately stop.
0AHEX	8AHEX	4AHEX	Decelerate and then stop.
10HEX	90HEX	50HEX	Start constant-speed operation at FL pulse rate.
11HEX	91HEX	51HEX	Start constant-speed operation at FH pulse rate.
13HEX	93HEX	53HEX	Start varied-speed operation.
14HEX	94HEX	54HEX	Output remaining pulses at FL pulse rate.
15HEX	95HEX	55HEX	Output remaining pulses at FH pulse rate.
17HEX	97HEX	57HEX	Output remaining pulses in varied-speed mode.
20HEX	A0HEX	60HEX	Suspend constant-speed operation at FL pulse rate.
21HEX	A1HEX	61HEX	Suspend constant-speed operation at FH pulse rate.
23HEX	A3HEX	63HEX	Suspend varied-speed operation.
24HEX	A4HEX	64HEX	Suspend output of remaining pulses at FL pulse rate.
25HEX	A5HEX	65HEX	Suspend output of remaining pulses at FH pulse rate.
27HEX	A7HEX	67HEX	Suspend output of remaining pulse in varied-speed mode.
30HEX	B0HEX	70HEX	Simultaneously start (no concern with axis designation).
38HEX	B8HEX	78HEX	Simultaneously stop (no concern with axis designation).

10.1.2 AP Output Control Commands (to Address 1 of Z80 Interface)



10.1.3 Bit Control Commands (to Address 2 of Z80 Interface)

Reset Commands			Set Commands			Subject Pins
a axis	b axis	a/b axes	a axis	b axis	a/b axes	
00HEX	80HEX	40HEX	20HEX	A0HEX	60HEX	General-purpose output pin AP0
01HEX	81HEX	41HEX	21HEX	A1HEX	61HEX	General-purpose output pin AP1
02HEX	82HEX	42HEX	22HEX	A2HEX	62HEX	General-purpose output pin AP2
03HEX	83HEX	43HEX	23HEX	A3HEX	63HEX	General-purpose output pin AP3
09HEX	89HEX	49HEX				Up/down counter clear
0AHEX	8AHEX	4AHEX				Deviation counter clear (out-of-step)
			2BHEX	ABHEX	6BHEX	Emergency stop

10.1.4 Register Control Commands (to Address 3 of Z80 Interface)

Read Commands		Write Commands		Subject Registers
a axis	b axis	a axis	b axis	
00HEX	80HEX	40HEX	C0HEX	R0 register (moving amount)
01HEX	81HEX	41HEX	C1HEX	R1 register (FL pulse rate)
02HEX	82HEX	42HEX	C2HEX	R2 register (FH pulse rate)
03HEX	83HEX	43HEX	C3HEX	R3 register (acceleration rate)
04HEX	84HEX	44HEX	C4HEX	R4 register (deceleration rate)
05HEX	85HEX	45HEX	C5HEX	R5 register (multiplication factor)
06HEX	86HEX	46HEX	C6HEX	R6 register (ramping-down point)
08HEX	88HEX	48HEX	C8HEX	R8 register (up/down counter)
09HEX	89HEX	49HEX	C9HEX	R9 register (environment setting 1)
0AHEX	8AHEX	4AHEX	CAHEX	R10 register (environment setting 2)
0BHEX	8BHEX	4BHEX	CBHEX	R11 register (environment setting 3)
0CHEX	8CHEX			R12 register (to read interrupt factor)
0DHEX	8DHEX			R13 register (to read counter value)
0EHEX	8EHEX			R14 register (command monitor)
0FHEX	8FHEX			R14 register (pin monitor)
3CHEX	BCHEX			Preset counter (to read counter value)
3DHEX	BDHEX			Ramping-down counter (to read counter value)
3FHEX	BFHEX	7FHEX	FFHEX	RMD register (to read or revise operation mode)

Caution: Never write any command other than listed above.

Notes of difference between PCL5023 and PCL5022

1. General information (matrix)

Items	**PCL5023**	**PCL5022**
1. Reference clock	19.6608 MHz (25 MHz max)	9.8304 MHz (10 MHz max)
2. Pulse rate setting steps	1 ~ 32767	1 ~ 16383
3. Max. output frequency	4.9 M pps (clock = 19.6608 MHz) 2.4 M pps (clock = 9.8304 MHz)	1.2 M pps (clock = 9.8304 MHz)
4. Acceleration/Deceleration mode	Linear and S curves	Linear
5. Accel setting range	1 ~ 65535	1 ~ 16383
6. Decel setting range	1 ~ 65535	1 ~ 16383
7. Accel S curve setting range	1 ~ 16383	Not available
8. Decel S curve setting range	1 ~ 16383	Not available
9. Ramp-down point setting range	0 ~ 16777215	0 ~ 4194303
10. Power requirement	5 V ± 10%	5 V ± 5%
11. Operating ambient temp.	- 30 ~ + 85 °C	0 ~ + 70 °C

2. Additional registers

PCL5023 has the following additional resisters compared with PCL5022.

A. R16(Register of acceleration S curve setting range)

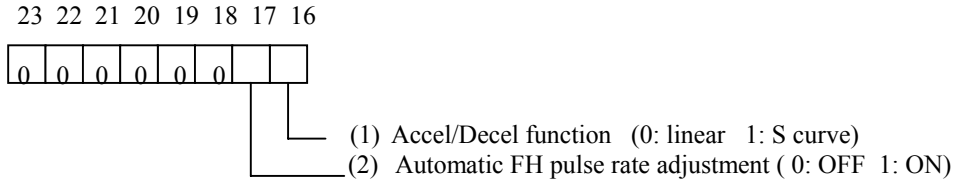
It controls S-curve setting range during acceleration. The setting range is 1 (0) ~ 16383. S-curve setting ranges during acceleration are (1) FL speed ~ (FL speed + R 16) and (2) (FH speed – R 16) ~ FH speed. Between ranges (1) and (2) is a linear acceleration. If you select 0 (default), PCL calculates internally and selects a value of (FH – FL) / 2.

B. R17(Register of deceleration S curve setting range)

It controls S-curve setting range during deceleration. The setting range is 1 (0) ~ 16383. S-curve setting ranges during deceleration are (1) FH speed ~ (FH speed - R 17) and (2) (FL speed + R 17) ~ FL speed. Between ranges (1) and (2) is a linear acceleration. If you select 0 (default), PCL calculates internally and selects a value of (FH – FL) / 2.

3. RMD (Operating mode register)

PCL5023 has 24 bit of RMD while PCL5022 has 16 bit. PCL5023's lower 16 bit has same function as PCL5022 does. Upper 8bit function is as follows:



(1) Accel/Decel function
Select linear accel/decel mode or S curve accel/decel mode. Default setting is for linear accel/decel mode.

(2) Automatic FH pulse rate adjustment
If the moving amount is too small in a programmable (preset) mode, the automatic ramp-down point setting function lowers the FH pulse rate to avoid a triangular profile.

4. Additional commands

The following commands are added for write/read of additional registers.

Read command	Read command	Write command	Write command	Descriptions
For a axis	For b axis	For a axis	For b axis	
10H	90H	50H	D0H	Read/Write of R16 register
11H	91H	51H	D1H	Read/Write of R17 register

5. Compatibility

A. Hardware

Package and pin positions of PCL5023 are same as these of PCL5022

B. Software

- Basically identical but please makes notes as follows:

When automatic ramping-down point setting is selected on PCL5023, acceleration and deceleration rate can be set independently on condition that R4 is equal or greater than R3. (PCL5022 only offers same acceleration rate and deceleration rate when automatic ramping-down point is selected). R4 value is always required for ramping-down point setting please set R4 value.

- Accel/decel time is different between linear profile and S curve profile. Here are equations.

Acceleration time of linear profile
Tul = (R2-R1) * (R3 +1) * 4 / Reference clock [Hz] (second)
Acceleration time of S curve profile
Tus= (R2-R1+R16*2) * (R3+1)*4 / Reference clock [Hz] (second)

R16 = 0, PCL calculates internally and selects a value of (FH – FL) / 2. Therefore
Tus= (R2-R1) * (R3+1)*8 / Reference clock [Hz] (second)
In this case, Tus = 2 x Tul

Deceleration time of linear profile
Tul = (R2-R1) * (R4 +1) * 4 / Reference clock [Hz] (second)
Deceleration time of S curve profile
Tus= (R2-R1+R17*2) * (R4+1)*4 / Reference clock [Hz] (second)

R17 = 0, PCL calculates internally and selects a value of (FH – FL) / 2. Therefore
Tus= (R2-R1) * (R4+1)*8 / Reference clock [Hz] (second)
In this case, Tus = 2 x Tul

- RMD register has 3 bytes.

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